Study on ambient gas effect in the annealing of ion-implanted GaAs toward realizing superior JFETs

（高性能 JFET 実現に向けたイオン注入 GaAs の
アニール時の雰囲気ガス効果に関する研究）

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THESIS

Study on ambient gas effect in the annealing of ion-implanted GaAs toward realizing superior JFETs

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Preface

The material of GaAs had inherently superior electronic properties, like extremely high electron mobility, large band gap, etc. However, the single crystal production technologies with excellent quality was not matured so that the controlling the crystal quality in the device fabrication process was quite important to extract the high potentiality of electronic properties. I was firstly in charge of the annealing of donor implanted GaAs toward the fully planar process GaAs FETs. The planer process was strongly recommended since it made followed interconnect formation process easier. The annealing temperature for the Si implanted GaAs attained to over 800 ºC and the suppression of dissolution of the As atoms in GaAs surface during annealing was fatal issue. The semi-insulating property of the GaAs was thought to be a result of compensation of C_{As} (C_{As} ; Carbon in As site) acceptor with EL2 (EL2 ; excess As related deep level) deep donor. A main p-type contamination was thought to be a C_{As} and V_{As} (V_{As} ; Vacancy in As site) fostered C_{As} at that time. Therefore, if the dissolution of As was happened the Si-donor activation must be lowered by C_{As} accepter. I employed the annealing method for ion implanted GaAs using AsH_3 for excess As over pressure based on H_2 carrier gas.

I was investigating the optimizing annealing condition for Si donor implanted GaAs in order to obtain higher activation day after day. The other day, I was noticed the difference between the C-V profiles of sample annealed in face-up method and that of face down method. The carrier profile annealed in face-up method is lower than that of face to face. In addition, the position of the profile of face-up method seemed to be slightly shifted to the direction of the surface. I felt this fact could not be explained by mere C_{As} formation. Some thought stroke on my head that some interaction with annealing ambient must be occurred in the surface. Then, I tried to execute annealing using Ar as another inert gas to confirm my intuition. The results were quite worthy because the activation efficiency were over 90% even in face-up method. I decided to clarify this cause in order to obtain stable and reproducible annealing for GaAs FETs.

The experiments were start with the investigation about the influence of H_2 gas on the activation of implanted Si. It was found that the activation efficiency, especially in face-up configuration, was clearly depends on the partial pressure of H_2 gas in H_2 / Ar gas mixture ambient. The carrier loss distribution in H_2 gas ambient and face-up configuration was estimated by comparing the carrier profile of the sample annealed in Ar ambient with that in H_2 ambient. As a result of that, it was found that some carrier compensating center distributed in the depth of 0.1-0.4μm, at the peak concentration of $1 - 2 \times 10^{16}$ cm^3.

As far as this carrier compensation center, it was thought to be a kind of defects or impurities which were induced in GaAs during H_2 ambient annealing. Firstly photoluminescence (PL) study was performed to investigate the origin of the carrier compensation. The properties of GaAs crystal at that time were thought to be a quite unstable in high temperature annealing and redistribution of many kinds of defects or impurities were reported. PL study was quite effective to identify the origin of carrier compensation since the depth of high sensitive region for PL study just coincided with that of carrier compensator. The Mn acceptor with activation energy of 100 meV was detected corresponding to H_2 partial pressure. In order to clarify the quantitative validity of Mn_{Ga} accumulation, SIMS analysis with step sputtering was performed under the cooperation of 'Surface Analysis Technology Gp' in SONY Research Center. As a result of that, the Mn_{Ga} accepter was detected in almost same amount and same depth of carrier compensator obtained by C-V measurement. Thus, the cause of lower carrier activation in Si-implanted GaAs in H_2 gas annealing was found to be due to Mn_{Ga} accumulation in the GaAs surface. However, it was still unclear that where the Mn derived from and what was the mechanism of Mn accumulation. Therefore, I determined to investigate the direct interaction of GaAs surface with H_2 gas like an 'etching phenomena'.

The experiments were performed to observe the difference of surface between uncovered region and covered region by protection film on the Si-implanted GaAs surface. The surface after annealing showed clear 'step' at the border between uncovered and covered region and this means 'etching' took place. The etching rate was found to be 1.0 – 1.5 nm / min. by measuring using 'Taly-step' and it was not depend on whether Si was implanted or not. In addition, the etching rate was proportional to the power of 2 third of H_2 partial pressure and not depended on the AsH_3 partial pressure. The activation energy of the etching was estimated to be 2.90 eV and it corresponded to the evaporation of Ga and that the surface after annealing showed mirror-like one. These results strongly implied that GaAs surface in the high temperature annealing under H_2 ambient was etched by H_2 gas congruently. Furthermore, this etching phenomenon was found to be cause of the Mn accumulation in the surface of GaAs. As far as the origin of the Mn itself it was concluded that it must be derived from not the outer contaminations but the bulk substrate existing as residual impurities because the extent of the accumulated Mn was deeply dependent on the lot or supplier makers of the GaAs wafer. This new finding impacted on not only the other electronic device fabrication process but also photonic devices fabrication like laser diodes since H_2 ambient had been used commonly and widely in the annealing or epitaxial growth process in order to avoid the oxidation at the surface.

Further details for the mechanism of Mn accumulation at the GaAs surface were studied by using semi-insulating GaAs substrate without Si ion implantation. The samples annealed in only H_2 ambient with or without AsH_3 showed p-type conversion. The SIMS analysis showed Mn accumulation in p-type converted samples at almost same quantity with carrier concentration measured by C-V method. However, Si atoms over the quantity of Mn were detected at the same time and the distribution of Si was quite similar to that of Mn. Normally, Si dopant in GaAs was said to occupy Ga site and to be Si_{Ga} as a donor although it was amphoteric atom. Although the Si must be related to the Mn accumulation from the similarity of the distribution profile of Mn and Si, Si should be no contribution for the conductive type. This fact required the Si must be an interstitial site or self-compensated by equivalent quantity of Si_{Ga} and Si_{As}. Therefore, it was to be a key issue to understand the mechanism of Mn accumulation that how the Si dopant behaved in GaAs during the high temperature was revealed.

The analysis method using 'channeling effect' in the crystal like RBS or PIXE is quite useful to know the crystallography or the occupied site of the impurities. I thought to utilize these analyses to investigate the occupied site determination of implanted or not implanted Si in GaAs. The collaboration with Professor Abe group in Hokkaido University was started since they had an ion accelerator of Vande Graff type and already reported so many good works in this field. It was concluded that the detected Si was not in interstitial site and Si seemed to be self-compensated by the site-transfer in the case with excess annealing. As a result of above experiment, the mechanism of Mn accumulation was thought to be a result of inter-diffusion in donor-accepter duplicated pair, for instance $Mn_{Ga}(-) – Si_{Ga}(+) – Si_{As}(-)$.

I established the new annealing method using Ar gas based ambient under the consideration of the disadvantages in H_2 gas ambient described above. The development of superior JFET was largely accelerated because reproducibility remarkably improved and also the turnaround time was effectively shortened by the annealing in face-up configuration. Especially, the dispersion of Vth in fabricated JFET in whole wafer and wafer to wafer was drastically improved. This fact was well explained by the suppression effect of the impurity re-distribution in Ar based annealing. This improved dispersion in Vth of JFET allowed the integration of large scale circuit. The maximum trans-conductance of 650 mS / mm and cut-off frequency of 65 GHz were accomplished. These were a level of worldwide record at that time. At the same time, the small scaled test circuit of a divide-by-four static frequency divider was fabricated and it proved the high potentiality of GaAs JFET by the operation at 6 GHz at the power consumption of 20 mW / flip-flop.

I faced so many difficulties and issues regarding the development of ICs, however, these were resolved one by one. These were, for instance, how to shorten the gate length,

how to control the Vth in Zn diffusion process, how to fabricate the Au based interconnect without damages, etc. After the GaAs JFETs developments in research center the technology was transferred to the business section. Firstly GaAs JFETs applied to the digital IC applications and some products were shipped. The demand for the ICs in the RF frontend of cellular phones was raised up meanwhile the fabrication processes of GaAs JFETs were sophisticated. So many designers who had a skill for RF circuit joined to me and a RF switches IC, a low noise amplifier and a power amplifier were started to develop. The good uniformity and the superior reproducibility with good cost effectiveness of GaAs JFETs were largely useful in these products development. Especially, simple plus voltage operation which was enabled by large forward bias of JFETs satisfied customer's demand so that the analog application of JFETs could took off favorably. Finally, I would like to describe that my work contributed in no small way to the success in GaAs IC business.

Contents

Chapter 1

Introduction

1.1 Aspects of GaAs devices for high-frequency and high speed applications

The semiconductor technology evolution shows no signs of stopping or slowing down. This is represented by so-called 'Moore's Law' and realized under the basis of the 'scaling principle' in CMOS devices. However, recently, CMOS technology started to weaken by its physical limits or economical reason. Accordingly, it is strongly said that the evolution must be taken not the direction of scaled down CMOS but that of functional integration. This movement is called as 'More than Moore' and system level integration is targeted. Therefore, it is getting more important to integrate the devices which cannot be ruled over by the "scaling", these are high-speed devices in analog circuit, various kinds of sensors, passive components, MEMS devices and so on. These devices will add the wide functions of systems and open the way to realize new products.

In recent circumstance, III-V compounds semiconductor represented by GaAs devices are still playing an important role in electronic systems. These are already getting standard devices in almost all wireless or wired communication front-end systems of mobile or stationary products like a Smart Phone, Tablet PC, TV-set etc. These network based products require extremely high-band width in order to treat high quality videos like HD or x4K and various kinds of data so-called "Big Data". This circumstance requires explosive evolution and spread in network communication. In order to widen or make thicken the capacity of the network, multi-band and/or multi-mode communication technologies have been developed and made them in use. In addition, various kinds of multiple coding technologies are invented and they require higher frequency in the carrier to expand the band utility. In these progress, compounds semiconductor devices are getting indispensable in the frontend of wireless and wired communication systems such as the power amplifiers, switches and low noise amplifiers in the micro-wave or millimeter wave RF systems, and also, laser drivers, receivers and ultra-high speed serial-parallel converters in the optical communication systems. The main reason is coming from that their superior characteristics and performance cannot be realized by Si CMOS devices.

Regarding the superior characteristics of GaAs FETs, for instance, RF switches

[1], power amplifiers [2], high speed digital applications [3, 4] and optical front-end ICs [5, 6] are already reported. These characteristics are mainly brought by the high performance of GaAs FET itself and they owed originally developed JFET (Junction FET) with superior performance by using original diffusion and annealing technology in ion-implanted GaAs. In order to apply this devices to actual IC or LSI products, the uniformity, reproducibility and/or production capability are essentially important factors in the JFET fabrication process adding to the superior performance in discrete devices.

1.2 A viewpoints of this work

The key factors to make success in consumer electronics are cost effectiveness and the performance. In order to achieve cost effectiveness, reproducibility, uniformity and productivity is especially important to raise the yield in fabrication process. In order to get superior performance, formation of shallow channel with higher carrier concentration in the FET is conclusively important as described in Chapter 2.2. The most simple and convenient method to make the active layers in the GaAs MES FET or JFET is ion-implantation and/or diffusion technique. These processes normally accompany high temperature treating above 600 °C - 900 °C. Therefore, thermal stabilities or properties of induced dopants, impurities, host atoms and/or various kinds of defects are essential concerns.

In addition, although the GaAs material is inherently having excellent electronic properties as described in Chapter 2.1, it is very difficult to control a stoichiometry in III-V compounds during the thermal treatment in the fabrication process since the each thermal properties of Ga and As is much different. As described in Chapter 3, various kinds of ideas or trials have been executed for the stoichiometric control of GaAs in the high temperature treating. However, unexpected carrier reduction or no reproducible incidents sometimes occurs. Therefore, it is fatal issue in so long time to realize excellent annealing method with no reduction in carrier activation and no diffusion in the interface between channel and bulk GaAs substrate.

Furthermore, it is also fatal issue to realize the excellent uniformity in FET characteristics in order to obtain the large scale integration with good yield. The GaAs substrate has a relatively large distribution of the defects or impurities that is induced in crystal growth process. These un-uniformity factors largely affect the deviation of FET characteristics, therefore, it is also fatal issue to suppress the redistribution of defects or impurities.

In this paper, I would describe the effect of annealing ambient in the donor activation process of ion-implanted GaAs. And then, it will be clarified by using the

electrical analysis (Hall measurements and C-V measurements), optical analysis (photoluminescence) and physical analysis (SIMS analysis and Q-mass analysis). In succession, the mechanism of the carrier compensation or redistribution is discussed by using the crystallographic analysis (RBS/PIXE method). On the basis of these findings, I proposed a new annealing method in the JFET fabrication. Finally, the superior JFETs with good uniformity are obtained and the superior high-speed operations are achieved in the high-speed test circuit fabricated by using the newly established annealing method I proposed.

Chapter 2

Backgrounds

2.1 Basic properties of GaAs

The basic GaAs characteristics compared with Ge and Si are shown in Table 1. The electrical and thermal characteristics of Si are excellent as shown in the Table 1, therefore, Ge transistor is replaced by Si. On the other hand, the main superior points in GaAs are higher electron mobility, larger band gap and so on. These are derived from its direct transition band structure. We should notice the each hole

Table 1 Important properties of Germanium (Ge), Silicon (Si) and Gallium Arsenide (GaAs) by A.S. Grove [7].

Materials	Ge	Si	GaAs
Atomic or molecular weight	72.6	28.09	144.63
Atoms or molecules /cm^3	4.42×10^{22}	5.00×10^{22}	2.3×10^{22}
Crystal structure	Diamond	Diamond	Zinc-blende
Lattice constant (nm)	5.66	5.43	5.65
Density (g/cm^3)	5.32	2.33	5.32
Energy gap (eV)	0.67	1.11	1.4
Effective density states			
Conduction band (cm^3)	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}
Valence band (cm^3)	6.0×10^{18}	1.04×10^{19}	7.0×10^{18}
Intrinsic carrier concentration (cm^3)	2.4×10^{18}	1.45×10^{10}	9×10^{6}
Intrinsic mobility (cm^2/v sec)			
electron	3900	1350	8600
hole	1900	480	250
Dielectric constant	16.3	11.7	12
Melting point (°C)	937	1415	1238
Vapor pressure (Torr)	10^{-7} at 880 °C	10^{-5} at 1250 °C	1 at 1050 °C
Specific heat (joule/g °C)	0.31	0.7	0.35
Thermal conductivity (watt/cm °C)	0.6	1.5	0.81
Coefficient of thermal expansion (1/ °C)	5.8×10^{-6}	2.5×10^{-6}	5.9×10^{-6}

mobility in Ge, Si and GaAs. The hole mobility of the GaAs is relatively smaller than that of Ge and Si so that the p-channel FET in GaAs is almost not developed so far. This fact means the complementary circuit like a Si CMOS cannot be realized in GaAs FET. This is one of the reasons that GaAs ICs do not target the low power digital ICs or LSIs.

As far as thermal property is concerned, a thermal conductivity and specific heat is also smaller than that of Si. In addition, vapor pressure in high temperature is much higher than that of Si and Ge as an order of 10^5. This is much different point with Si and this means meticulous attention must be paid for desorption of GaAs host atoms in the high temperature treatment. This is the one of the main reasons for the difficulties in the fabrication process of GaAs FETs.

The crystal structure of GaAs is zinc-blende structure as shown in Figure 1. Normally, GaAs substrate is obtained by the cutting and the thinning of the ingot produced by using LEC (Liquid Encapsulated Czochralski) method or HB (Horizontal Bridgeman) method. In the LEC growing method, excess As is added into the PBN (Periotic Boron Nitride) crucible with Ga and As poly-crystal in order to avoid dissolution of arsenic molecular. It is well known that this excess arsenic atom formed the deep level (It is called as EL2) in GaAs, as a consequence, LEC grown GaAs shows semi-insulating properties [8, 9]. In the HB grown method, major contamination is Si shallow donor, coming from silica boat so that substrate shows inherently n-type. Cr metal, as a deep acceptor, is intentionally doped in order to obtain semi-insulating property.

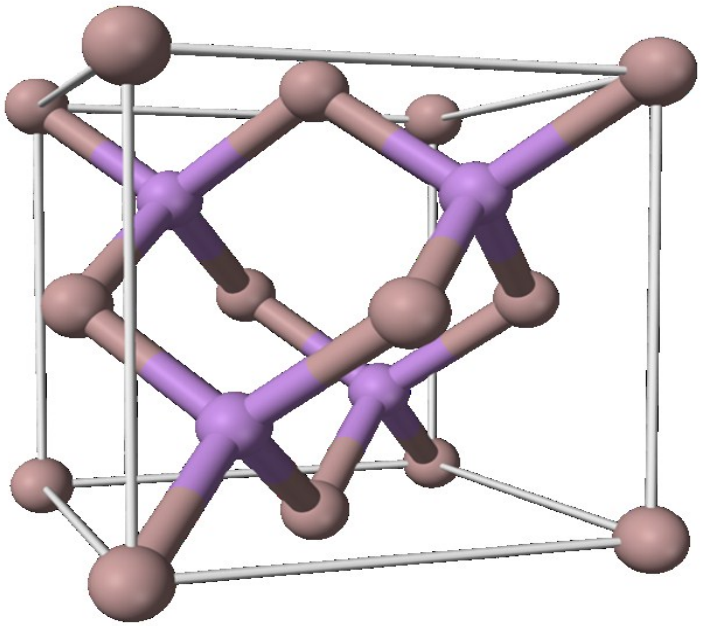

Figure 1: GaAs Zinc-blende crystal structure.

This semi-insulating property is quite convenient for making ICs because there is no necessity to make isolation area. However, the semi-insulating properties cause some serious problems in thermal stabilities or electrical properties. As far as the electrical instability is concerned, high electrical field will be generated between the gate or source region and the neighbor drain region when the distance between the FET and neighbor FET is small. As a consequence, the region between the both transistor will be conductive by the carrier comes from the collapsed compensated state. This phenomenon is so-called 'side gating effect' or 'back gating effect' and the layout of each transistor must be paid much attention, otherwise proper isolation method must be required [10]. Regarding thermal stability issue, p-type or n-type conversion sometimes takes place at the surface of GaAs after the annealing over 800 °C. The origin of this type conversion is said to be the result of breaking of carrier compensation. N-type conversion at the surface in HB grown Cr-doped substrate, for instance, is said to be the results of Cr out-diffusion by thermal treatment [10]. P-type conversion in the un-dope LEC grown substrate is said to be the result of breakout of various kinds of compensation relation. P-type conversion especially in H_2 ambient annealing is one of the issues in this paper and it will be investigated in detail and discussed in Chapter 6.

The properties of the thermal instability in the ion-implanted GaAs is more complicated than that of bulk semi-insulating GaAs. The lattice structure of the host crystal is destroyed into a disordered or an amorphous state. This means the various kinds of defects or dislocations must be induced by the ion-implantation process. Therefore, the crystal structure restoring process in the high temperature annealing after ion implantation is investigated by using RBS/PIXE analysis. These analyses are based on the nature of the 'channeling' in the crystal structure. A representative channeling views in the GaAs case is shown in Figure 2. The various kinds of information in crystal can be obtained by utilizing this channeling effect. The detail results are described in Chapter 7 and some important findings are revealed.

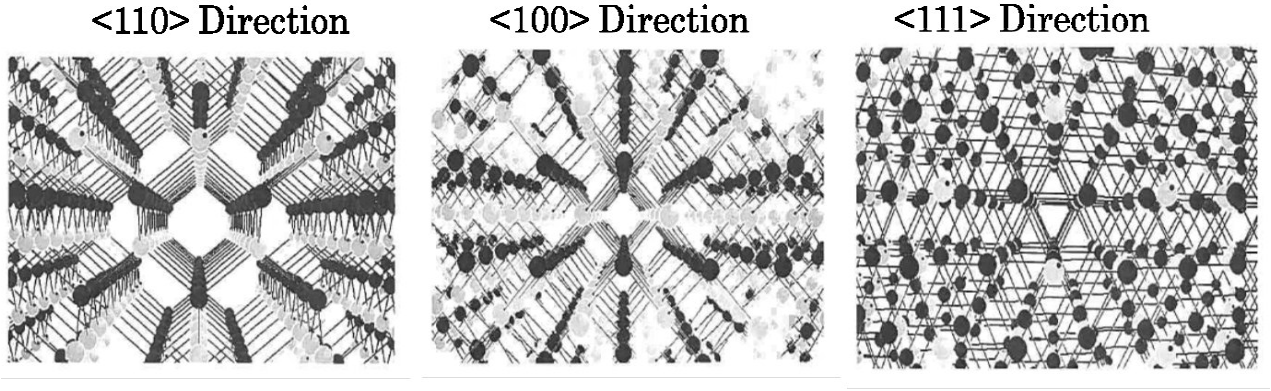

Figure 2: Perspective view in GaAs crystal from each direction.

2.2 A theory for FETs and ICs

Various approaches to make MOS FET in GaAs have been investigated on the basis of Si MOS FET structure in the past. However, it has been found the oxidation with excellent quality in the GaAs surface is quite difficult to obtain. Therefore, different structures suit for GaAs properties are energetically investigated. These are MES FET, JFET and Hetero Structured FET. Schematic views of 3 types FET are shown in Figure 3(a), 3(b) and 3(c). The band diagram of each FET is likewise shown in Figure 4(a), 4(b) and 4(c). MES FET is most popular device in GaAs and the channel, source and drain region are normally formed by using selective ion implantation and annealing. The gate is structured by using Metal-Semiconductor Schottky barrier. The limits of the forward gate bias *Vf* is determined by the work function ϕ_B of the gate metal as is shown in the Figure 4(a). The metal commonly used for MES FET is Al or Au and *Vf* is order of 0.7～0.8V. This small *Vf* is to be a disadvantage when a large gain in the wide bias voltage range is required. In addition, cleanness of the surface and the damage-less fabrication process must be taken care to obtain the good and stable Schottky gate.

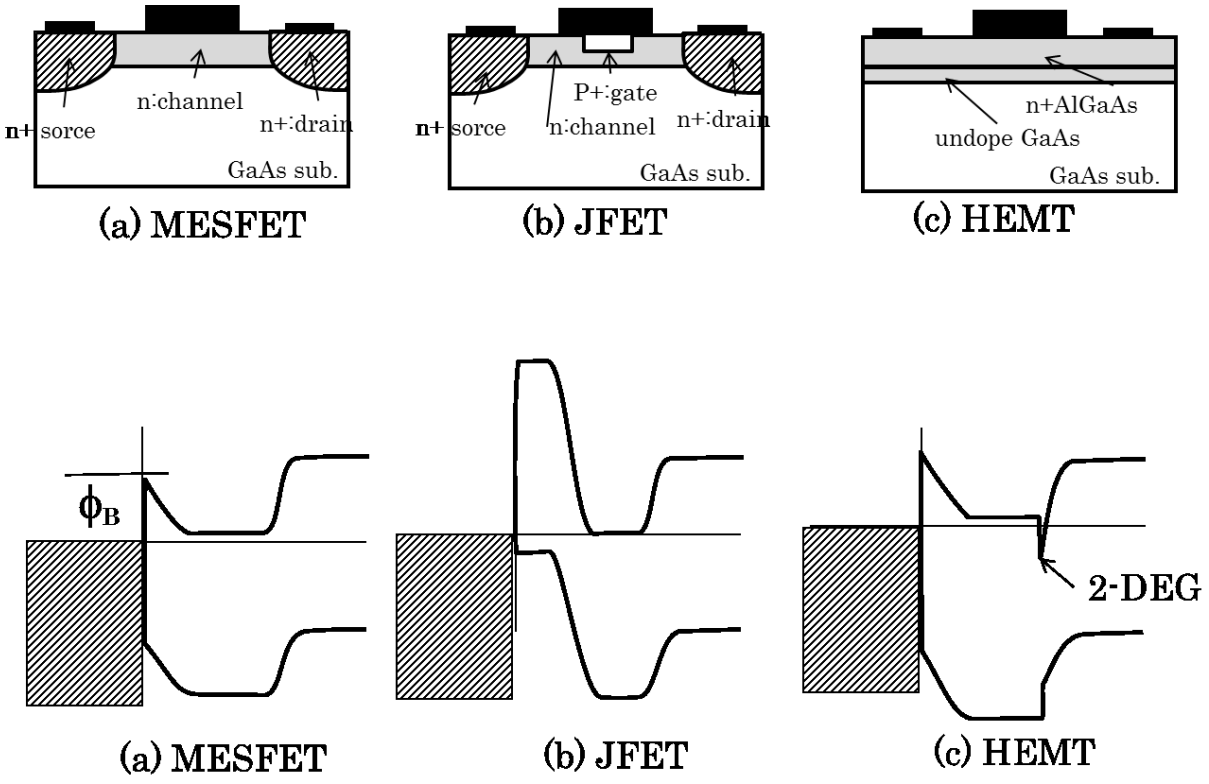

Figure 4: Band diagram of representive GaAs FETs.

On the other hand, JFET structure is also proposed in order to overcome the weak points of MESFET. The gate structure bases on a p-n junction, therefore, we can obtain larger *Vf* up to band-gap energy of 1.4 eV in the GaAs case as shown in Figure 4(b). The formation technology of p-type layer is one of the key issues. The stable formation of p-type layer using Zn diffusion into the Si implanted n-type GaAs substrate is already achieved under the arsenic overpressure by M. Dosen [12]. The *Vf* of the JFET is about 1.4V, therefore, high gain in the wide bias voltage is possible. At the same time, enhancement mode FET operation with high gain can be easily achieved in the JFET structure. It means that circuit operation in only + voltage power supply is possible and this will be a large advantage for the consumer products application. This advantage is to be one of the key factors to win the business in the RF-applications like RF switches or amplifiers.

As far as a hetero structured FET concerned, so many kinds of hetero FETs have been investigated and proposed. The most important device is a so-called HEMT (High-Electron Mobility-Transistor) based on an $Al_{0.3}Ga_{0.7}As$/GaAs hetero interface. The composition of 0.3 in Al and 0.7 in Ga is chosen as Al_xGa_yAs lattice constant matched with that of GaAs. The evolution of the epitaxial growth technology like a MBE (Molecular Beam Epitaxy) or a MOCVD (Metal Organic Chemical Vapor Deposition) allows various kinds of the composition of not only the III-V compounds but also II-VI. The abrupt interface with good quality is obtained by the advanced crystal growth technologies mentioned above so that various kinds of artificial structure are accomplished like a 'Quantum Well' or 'Quantum Dot'. These artificial structures bring drastic improvement not only in the electrical properties but also the optical properties. The name of the HEMT is derived from the 2 dimensional electron gas (2DEG). The principle of the HEMT is explained as bellows. As shown in Figure 4(c) the triangle well is formed in the hetero interface of un-doped GaAs side, so that the carrier in the n-type AlGaAs is spill over into the triangle well. Marvelous high electron mobility is obtained in this structure by virtue of the avoidance of impurities based electron scattering. This structure can be applied to the composition of the various kinds of materials. Pseudmorphic HEMT consists of AlGaAs/InGaAs/GaAs structure, for instance, is a representative device which is using the effect of intentional strain in the channel. This strain induces the breakout of degeneration in valence band structure so that the hole mobility can bring up. However, a reliability or thermal stability of the strained channel is thought to be one of the issues [13].

By cooling down to 77 K the electron mobility raises over 200,000 cm / sec [14], therefore, HEMT devices well match with ultra-low noise applications like a radio telescope or aero-space communications. On the other hand, these devices are not to

be commonly used in the consumer products by means of complicated fabrication process like an additional isolation process and necessity of cooling in the use of superior operation.

Therefore, the JFET is selected and developed as a candidate for the basic FET for ICs. However, the findings or results described in this paper, of course, can be applied to fabricate other kinds of FETs and ICs.

2.3 Issues for the superior electronic device

In this chapter the structural requirements will be discussed from the viewpoints of realizing a superior performance in the JFET. In the performance of FETs one of the representative figures of performance is f_T (f_T; cut off frequency). f_T indicate maximum frequency limit of operation, and it will be written as;

$$f_T = 1/2\pi T$$
$$= v_{eff} / 2\pi Lg$$
$$= G_m / 2\pi\, CgWgLg \qquad (1)$$

Here, G_m is a trans-conductance and indicates a rate of variability of drain current toward the gate bias voltage and v_{eff} is an average velocity of electron. Lg=gate length, Wg=gate width and Cg is capacitance around the gate, normally, Cg=Cgs (capacitance between gate and source electrode) + Cgd (capacitance between gate and drain electrode). Therefore, the meaning of the equation (1) is f_T corresponds to a reverse of the flight time of electron in the channel or charging time of the Cg by the drain current. Normally G_m is represented by using G_{mi} and Rs as follows;

$$G_m = G_{mi} / (1+ G_{mi}\, Rs) \qquad (2)$$

Here, G_{mi} is an intrinsic trans-conductance and it means a kind of conductance between the channel and source electrode region and Rs is a resistance in source region. From the equation, it is easily understood that higher G_m and lower Cg brings superior high frequency performance. In order to obtain higher G_m, higher carrier concentration and electron mobility in the channel of FET are essentially required.

Furthermore, the G_m is also expressed by below equation from the Shockley JFET model [7];

$$G_m = W_G * \mu * \varepsilon (V_G - V_{th}) / L_a * L_G \qquad (3)$$

Here, L_a = channel thickness, μ = electron mobility, ε = dielectric constant of the GaAs, V_G = gate bias voltage and V_{th} = threshold voltage.

This implies that the carrier distribution in the channel must be shallow and

peak concentration must be higher. This fact means that we have to obtain the shallow and the highly activated channel without any carrier compensation through the ion implantation and the annealing. Although the various kinds of thermal treatment are experienced in the JFET fabrication process as described in Chapter 7.2, especially, the annealing for the activation of implanted Si donor is the highest temperature process. The annealing temperature normally attain to over 800 °C, so that the dissolution issues at the surface of GaAs should be maximally taken care. In the next Chapter, previous works for ion implantation and annealing in GaAs are explained and the difficulties in each annealing methods will be described with its reason.

Chapter 3

Previous work for ion implantation and annealing of GaAs

3.1 Ion implantation in GaAs

Generally speaking ion-implantation technology is so often used for semiconductor devices. Important factors are implantation energy and dose and the dopant distribution profile. The dopant profile is to be a Gaussian distribution if the host material is homogeneous substance as is calculated by LSS (Lindhard, Scharff, Schiott Theory) theory [15]. The incident angle of ion beam must be selected as avoiding the channeling direction in order to obtain the stable and reproducible distribution of the dopant. As described in Chapter 1 (100) oriented surface is normally used for GaAs substrate so that the substrate is set with some tilt and rotate angle during ion implantation in order to avoid the channeling effect [16]. The energy level of the various kinds of dopants in GaAs is already investigated and summarized well in detail by S. M. Sze [17]. Si or Se is normally used as n-type dopant and C, Zn, or Be is used for p-type dopant. In this paper all the experiments are performed by using Si as a n-type dopant within the energy range of 60 keV - 160 keV and in the dose range of 10^{12} cm^{-2} - 10^{16} cm^{-2}. The implantation energy and the dose are changed as matching with purpose of each experiment. It is a main reason for using Si dopant that Si is a relatively stable during annealing and also has a no toxic characteristics. After Si implantation into the GaAs substrate an annealing is performed. The implanted Si re-distributes in the GaAs substrate affecting by the various conditions in the annealing. These affecting factors are, for instance, annealing temperature, time, ambient, heating method, heating rate, a configuration for setup, and so on. The activation ratio is defined by the ratio of the Si_{Ga} (Si in Ga site) to the whole implanted Si.

3.2 Cap annealing and capless annealing

It is well known that 'Cap Annealing' and 'Capless Annealing' are investigated in order to avoid the dissolution of GaAs in the high temperature annealing. In the 'Cap Annealing', Si_3N_4, SiO_2 or SiN_xO_{1-x} films are typically used as a protection layer [18].

The cap layer is normally deposited after Si donor implanted by low temperature plasma CVD (p-CVD) method in the temperature range of 300 - 400 °C. This capped GaAs substrate is annealed in the N_2/H_2 or Ar/H_2 mixture gas in the temperature range of 800 - 950 °C. Unless the quality of the protection layer is void-less and non-defective, a pealing or a cracking of protection layer takes place so often. The protection films of SiO_x or SiN_y have a residual stress at the interface with GaAs surface so that it causes sometime unexpected diffusion of the dopant and/or host

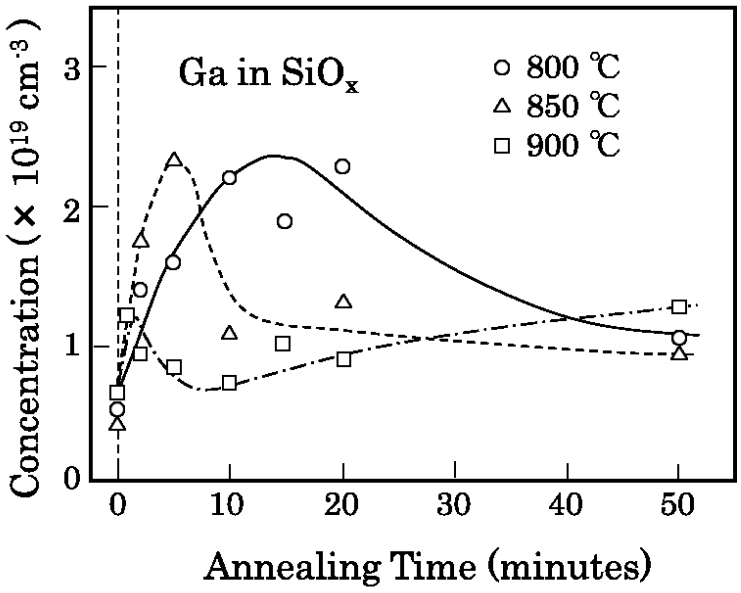

Figure 5: Residual Ga atoms in SiO_x films as functions of annealing time and temperature.

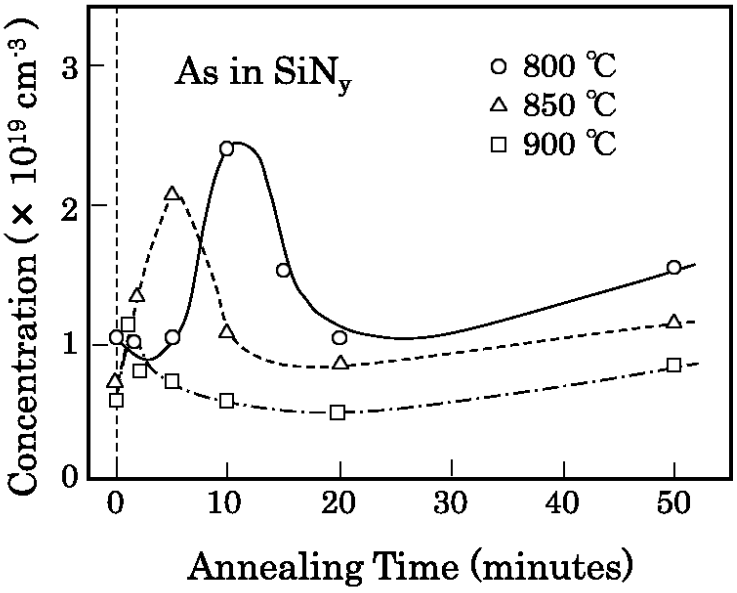

Figure 6: Residual As atoms in SiN_y films as functions of annealing time and temperature.

atoms. The quality of the protection film can be controlled by controlling the quantity of hydrogen atoms which is incorporated in the p-CVD process. However, it is found that the Ga or As atoms diffused into the protection films during the annealing even if the good quality in the protection layer obtained. In addition, the damaged layer in surface is induced by the film deposition process resulting in the anomalous diffusion takes place in the protection layer [19]. Here, only the results of out-diffusion introduced in Figure 5 and 6. For the details about this out-diffusion phenomena please see the APPENDIX I. Although it is remarkable results, the Ga out-diffusion in SiO_x film mainly occurs, on the contrary, the As out-diffusion in SiN film mainly does. Figure 5 shows the results of out-diffusion of Ga in SiO_x / GaAs system and Figure 6 shows that of As in SiN_y / GaAs system evaluated by RBS/PIXE analysis. The properties of out-diffusion of each atoms are quite anomalous, namely, the quantity of residual host atoms of Ga and As in both films of SiO_x or SiN_y shows peaks in short annealing time. This peak goes away by the further annealing in time. These phenomena can be explained by the model that some damaged layer existing in GaAs surface will diffused into protect film at first, and then, the host atoms gradually out diffuse. The damaged layer is thought to be induced in the process of protect film deposition. The thermal CVD at 400 °C and the p-CVD at 350 °C are used for SiO_x and SiN_y film deposition, respectively. Therefore, a different kind of damaged layer is thought to be induced in each surface of GaAs. Thus the properties of out diffusion in capped annealing strongly affected by the state of interface in protect film and GaAs surface.

Furthermore, this capping layer give a residual stress for GaAs substrate especially near in the surface because the difference of thermal coefficient is large between capping layer and GaAs. This stress sometimes brings an anomalous

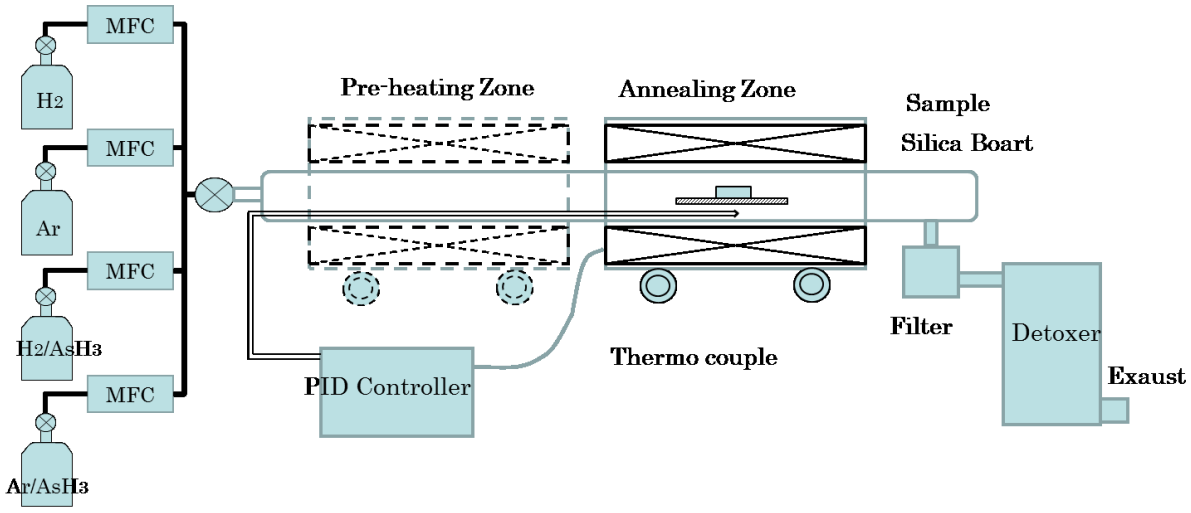

Figure 7: Schematic view of annealing apparatus.

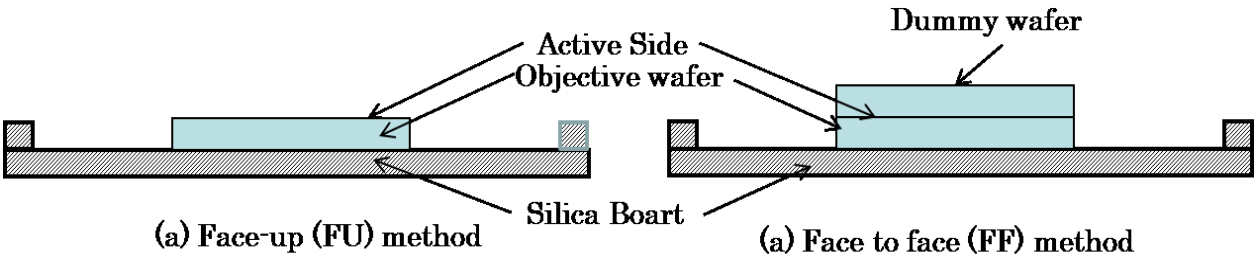

Figure 8: Wafer set-up configurations.

diffusion of the implanted dopant. Thus this method is quite sensitive for the deposition condition of capping layer so that it is extremely difficult to archive a good uniformity and good reproducibility in the activation of the implanted dopant for GaAs.

Therefore, the 'capless anneal' method is proposed by J. Kasahara et. al. [20] A capless anneal is performed in the As over pressure which is induced by AsH_3 gas instead of the film protection. The induced AsH_3 dissolved in the furnace into As_2 and H_2 perfectly resulted in As over pressure is applied. A schematic view of the annealing apparatus is shown in Figure 7. The furnace is on the rail and it can be move from the pre-heating zone to the annealing zone. An excess AsH_3 or As is collect in the detox apparatus equipped at the end of the furnace. The temperature is controlled by PID controller by detecting the temperature using the thermocouple set inside in quartzes tube. The radius of the quartzes tube is about 12 cm and 2 or 3 inch GaAs wafer can be annealed. After ion implantation samples are set on a quartz boat horizontally with both holding configurations of Face-up (FU) and the Face to Face (FF) method. Here the FF method is a configuration that the objective wafer is covered with another GaAs wafer as illustrated in Figure 8.

An H_2 ambient gas is chosen as a carrier gas since the surface of GaAs has to be protected from oxidation or contamination during high temperature annealing. The partial pressure of AsH_3 is determined by controlling the flow ratio of AsH_3 and H_2. The typical partial pressure of AsH_3 is 3 Torr which is calculated under the assumption of total pressure is approximately 760 Torr because the furnace is open type.

The basic electrical properties are evaluated by using Van Der Paw method for Hall measurement and Hg Schottky probe method for C-V measurement after the annealing. The samples are cut into 5 mm□ under the consideration of wafer orientation. Indium dot of the order of 1 mm in diameter are put on the four corners of the samples and an ohmic contact is made by alloying in forming gas at the condition of 400 °C / several seconds.

In the typical annealing condition, as is 100 % H_2/AsH_3 annealing, activation

ratio is investigated in both configuration of Face-up and Face to Face. The used dopant for n-type is Si and the implantation with accelerate energy of 130 keV and with dose of 3×10^{12} cm^{-2} are performed.

The electrical properties of sheet carrier density N_s (cm^{-2}), sheet resistance ρ_s ($\Omega/\square$), Hall mobility μ ($cm^2/V \cdot sec$) obtained by Hall measurement and calculated activate ratio are shown in Table 2. Activation ratio in Table 2 is calculated from the following C-V measurement by integrating the carrier profile. As easily understanding, the activation ratio with FU method is about 68 % and even that with FF method is 86 %. The difference between the FU method and the FF method is relatively large. The carrier profiles in both cases measured by C-V method are shown in Figure 9. The profile of FU configuration is explicitly low in peak and slender in depth than FF configuration. The annealing results in FF method might be acceptable in the view points of activation ratio, however, the FF method should be avoided from the production cost because the twice quantity of GaAs substrate will be consumed at a once and the flexibility of the set up configuration like a vertically set-up batch processing must be lost.

The poor activation ratio, especially in FU configuration, is indicating some unexpected interaction between H_2 and GaAs surface since the profile of FU configuration in Figure 9 is excessively slender than that of FF configuration. In order to investigate the cause of the lower activation ratio in H_2/AsH_3 annealing, especially in FU method, carrier ambient gas dependency on the activation of Si in GaAs is carefully studied.

Table 2: Results of Hall measurement for the samples annealed in H_2 carrier gas.

Carrier Gas	Set-up	P_{AsH3} (Torr)	P_{H2} (Torr)	ρs ($\Omega/\square$)	Ns (cm^{-2})	μ ($cm^2/V \cdot sec$)	η (%)
H_2	FU	3	760	1.09×10^3	1.67×10^{12}	3611	68
H_2	FF	3	760	8.15×10^2	1.99×10^{12}	3893	85

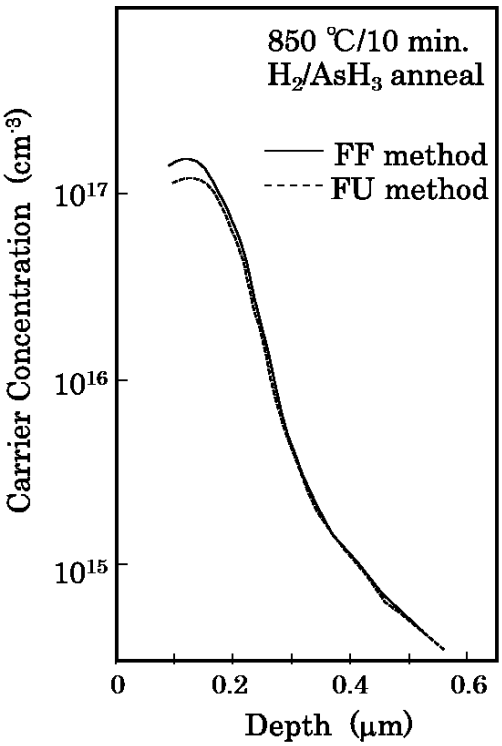

Figure 9 : Carierr profiles in H_2/AsH_3 annealing measured by Hg probe C-V method.

Chapter 4

Ambient gas effect on activation of Si ion-implanted GaAs

4.1 Sample preparation

The samples to be ion implanted are first degreased and chemically etched to remove native oxide and contaminations. The used samples are same as in Chapter 3.2, namely, the used dopant for n-type is Si and the implantation with accelerate energy of 130 keV and with dose of 3×10^{12} cm^{-2} are performed. After ion implantation samples are set on a quartz boat horizontally with both holding configurations of Face-up (FU) and the Face to Face (FF) method. In order to investigate the ambient gas dependency, annealing experiments are performed under the condition of varying the partial pressure of Ar and H_2. Specifically, the partial pressure is changed by changing a flow ratio of Ar and H_2. Here, the total flow rate keeps at 0.5 l/sec. Typical annealing condition is 850 °C in anneal temperature and 10 minutes in anneal time. Not only the dependency of atmosphere but also that of annealing temperature, time and AsH_3 partial pressure is also investigated.

The basic electrical properties are evaluated by also using Van Der Paw method for Hall measurement and Hg Schottky probe method for C-V measurement.

4.2 Influence of the carrier ambient gas

The Ar gas is chosen as a carrier gas because Ar is one of the inert gases and very popular as a forming gas. Furthermore, molecular weight of Ar is 40 and this is much closer to that of AsH_3 (molecular weight is 78) than H_2. This means better gas mixture state is easily obtained. In addition, N_2 gas should be avoided because there is a possibility of direct reaction with GaAs since N_2 is a group V elements. The annealing with 100% Ar/AsH_3 ambient is executed and the results are shown in Table 3. It is easily understanding that the activation ratio of the Ar 100 % annealing is higher than that of H_2 100 % especially in a FU configuration. This fact explicitly suggests that some interaction factors exist between H_2 gas and GaAs surface.

Table 3: Results of Hall measurement for the samples annealed in Ar carrier gas.

Carrier Gas	Set-up	P_{AsH3} (Torr)	P_{H2} (Torr)	ρs (Ω/□)	Ns (cm^{-2})	μ ($cm^2/V\cdot sec$)	η (%)
Ar	FU	3	0	7.33×10^2	2.12×10^{12}	4016	91
Ar	FF	3	0	7.01×10^2	2.17×10^{12}	4122	96

The carrier distribution profiles by C-V measurement in the Ar cases are shown in Figure 10. The profile in Ar 100 % annealing shows a little bit higher peak carrier concentration and slightly fat in depth distribution than that of H_2 100 % annealing. The difference in activation ratio between both samples is well explained by the difference between both carrier profiles. Furthermore, the fact that the activation ratio only in FU case of 100 % H_2 annealing is prominently worse strongly indicates something happen in annealing of H_2 atmosphere.

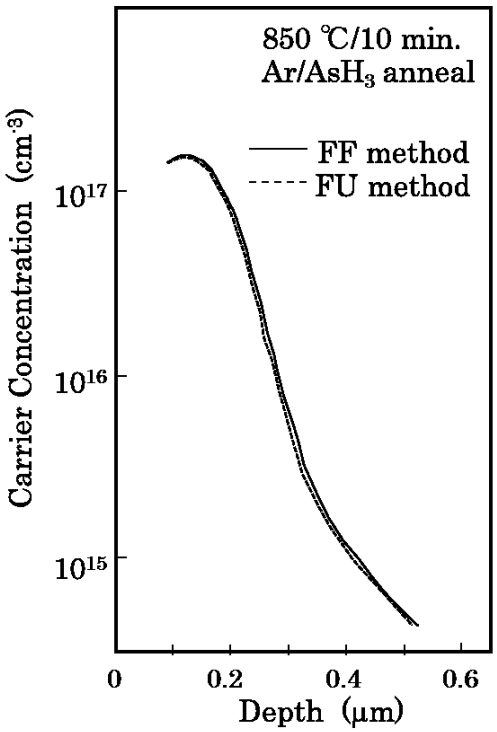

Figure 10: Carierr profiles in Ar/AsH_3 annealing

In order to investigate the effects of Ar ambient annealing the H_2/Ar partial pressure in $Ar/H_2/AsH_3$ annealing is intentionally changed. In all the experiments the partial pressure of AsH_3 keeps constant at 3 Torr and the partial pressure of H_2 is varied by changing the Ar mixture ratio in carrier gas with the both setting of FU and FF configuration. The measured electrical properties Ns, μ and ρ_s are

summarized in Figure 11. The Ns and μ are increasing as the H_2 partial pressure is decreasing and the ρ_s is decreasing on the contrary. These facts apparently indicate the carrier reduction in activation is getting larger as increasing the partial of H_2 ambient. The carrier profiles change measured by C-V method is shown in Figure 12. The peak carrier concentration is getting smaller and the depth profile is getting slender according to the H_2 partial pressure increasing.

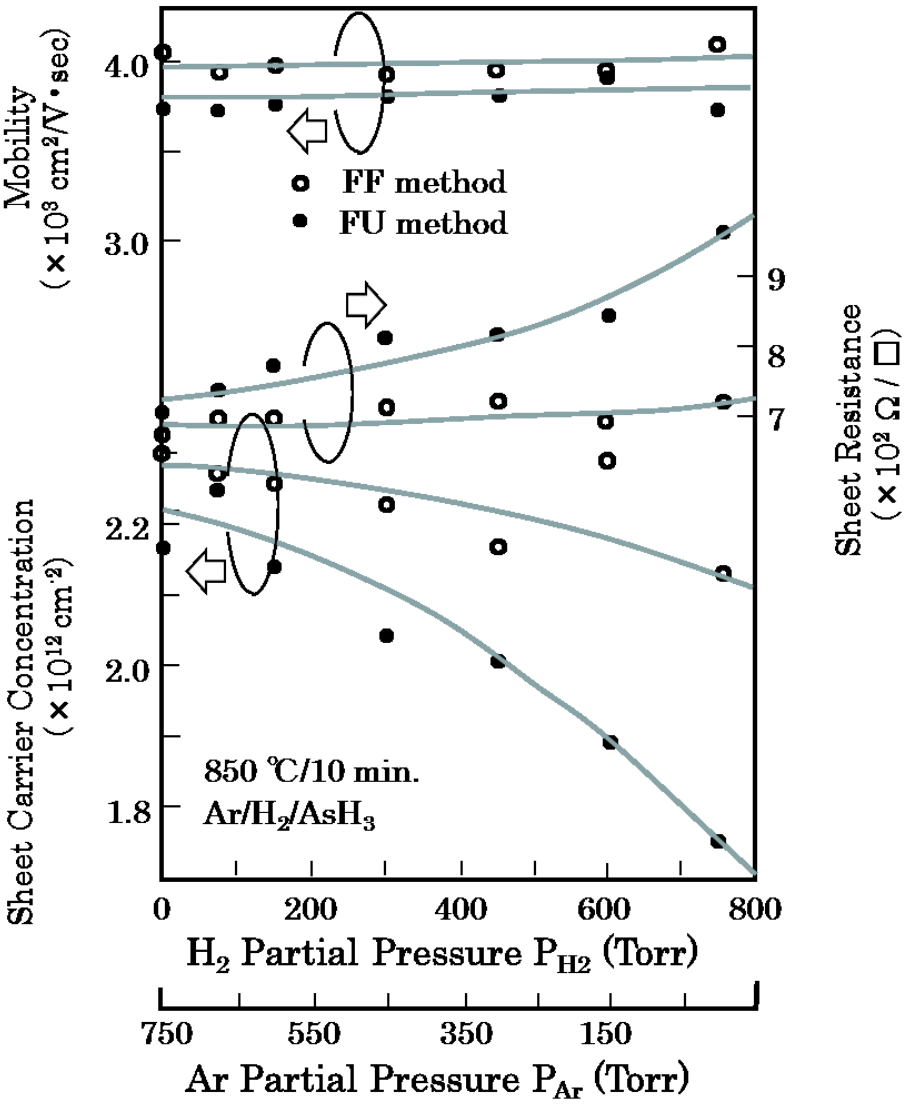

Figure 11: P_{H_2} dependency of Ns, ρ and μ obtained by Hall measurement.

Net lost carrier concentration is calculated by extracting the profile of the Ar annealing from that of the H_2 annealing. The results are shown in Figure 13 and it will indicate that there is something to be a cause of carrier lost existing near the surface. The peak concentration of the lost carrier is estimated about the order of 2 - 3 $\times 10^{16}$ cm^{-3} and the depth attains to the order of 300-400 nm.

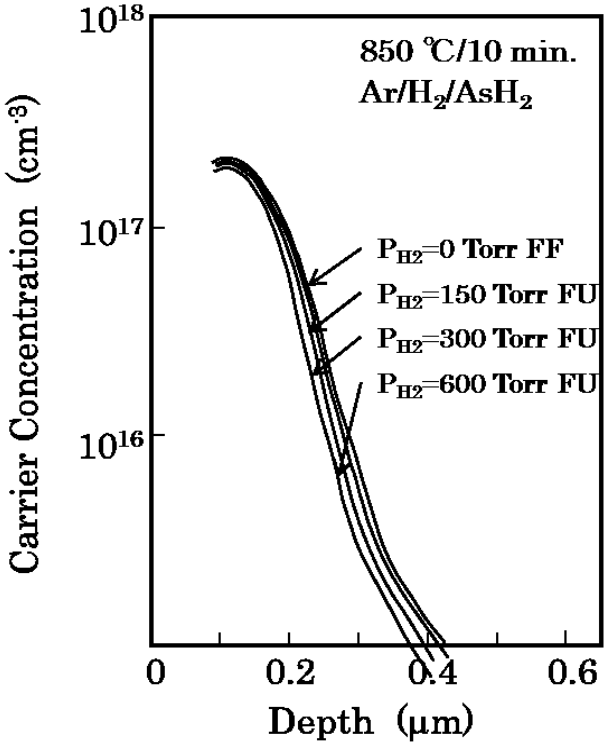

Figure 12: P_{H2} dependency of carrier profiles by C-V measurement.

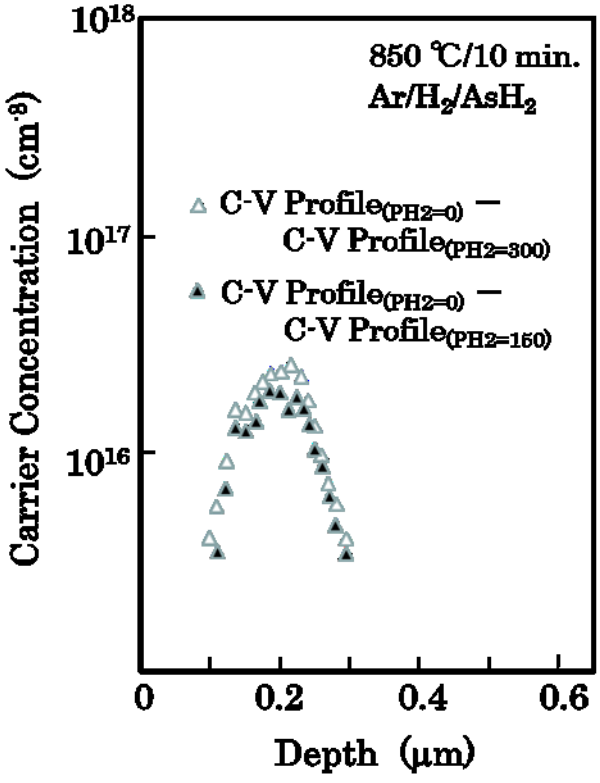

Figure 13: Lost carrier distribution near the surface.

4.3 Impurity pile-up on the surface

In order to investigate the cause of carrier lost near the surface photoluminescence studies are performed. If the cause of carrier lost is due to formation of some defect or a kind of impurities redistribution, photoluminescence study is adequately effective since the penetration depth of the excitation light is as same as the depth of lost carrier distribution. Photoluminescence study is executed in following conditions;

Ar Gas Laser at 514.5 nm is used as an excitation light source and photo multiplier (Hamamatsu Photonics Co.) is used as a light detector. The measuring temperature is determined to be at 4.2 K because the various structural change or luminescence from the re-combination center induced by some impurities should be de-convolved clearly.

Firstly the photoluminescence spectrum measurement in the case of 100 % Ar/AsH_3 ambient annealing is performed and the result is shown in Figure 14. The distinct luminescence peaks are seen around the energy level of 1.51 eV, 1.49 eV, 1.43 eV and 1.41 eV. The origin of the each peak is already investigated in detail [21, 22] so that the luminescence peaks around the 1.51 eV, 1.49 eV, 1.43 eV and 1.41 eV are identified as the band edge emission, C_{As} acceptor related emission, 1LO phonon replica of C_{As} related peak and Mn_{Ga} related emission respectively. The peaks around

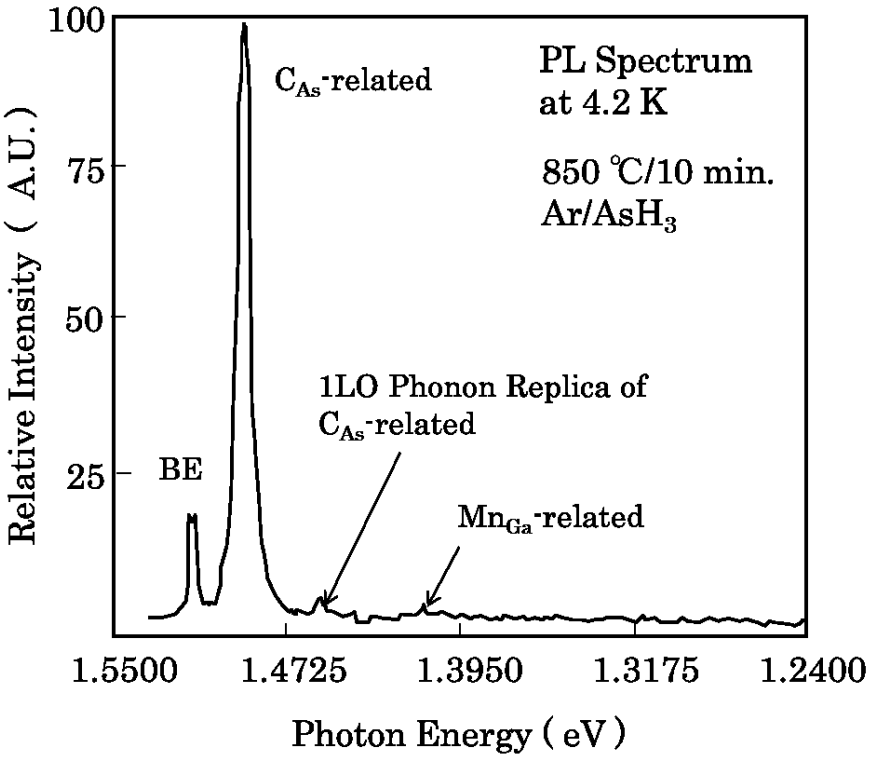

Figure 14: Typical photoluminescense spectrum in Ar 100 % annealing.

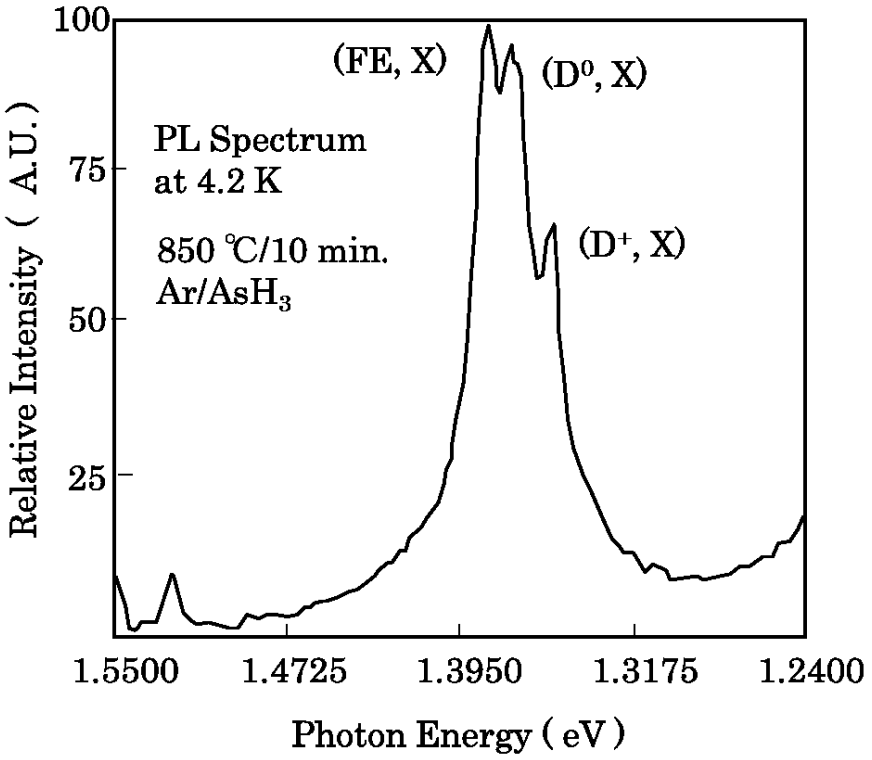

Figure 15: Photoluminescence spectrum near band edge.

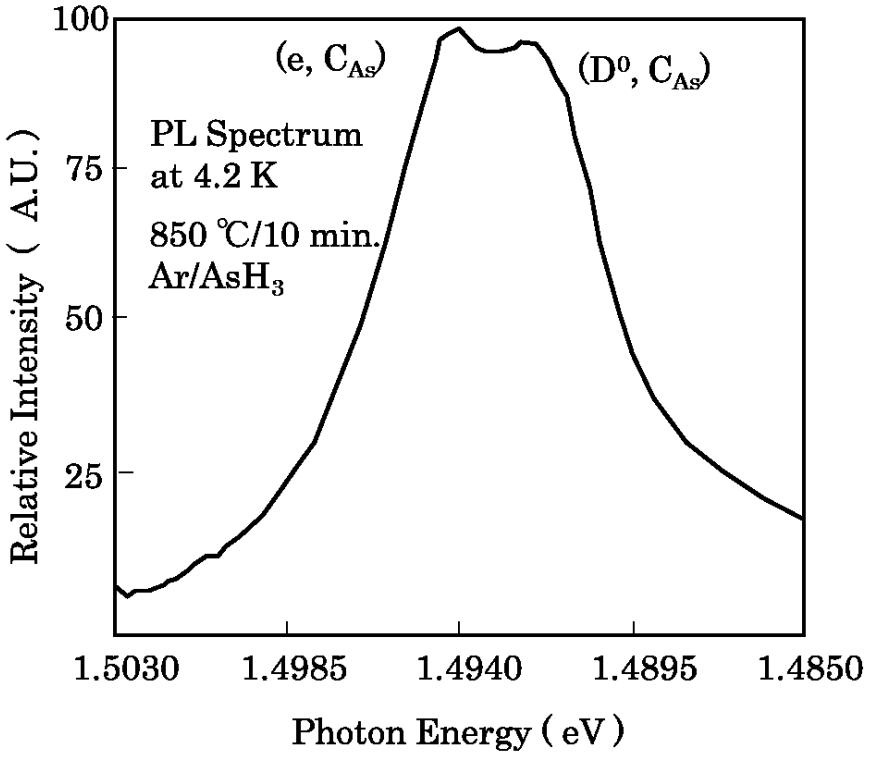

Figure 16: Photoluminescence spectrum near 1.49 eV.

the 1.51 eV and 1.49 eV are enlarged in Figure 15 and 16, respectively. The peaks around 1.51 eV including 3 peaks at 1.5161 eV, 1.5152 eV and 1.5135 eV as shown in Figure 15. These peaks are exciton related peaks of (Free Exciton), (D_0, Exiton), (D+, Exciton) respectively. The peaks near the 1.49eV also including 2 peaks at 1.4943 eV and 1.4924 eV as shown in Figure 16 and they are estimated to be C_{As} acceptor related peaks of (e, C_{As}) and (D_0, C_{As}). In these luminescence peaks, the change of the peak of the C_{As} related and that of the Mn_{Ga} related must be carefully looked at because the both are estimated to act as an acceptor in GaAs [16] and it will be a candidate of carrier loss.

The H_2 partial pressure dependency of the photoluminescence is investigated based on the basic luminescence properties identified above. The change of the photoluminescence property according to the changing of the H_2 partial pressure is shown in Figure 17. The peaks around the 1.41 eV are drastically increasing as the partial pressure of H_2 increasing. The peak at 1.412 eV of Mn_{Ga} acceptor as explained above accompanies 2 other peaks of 1.378 eV and 1.340 eV. They are estimated to be a 1LO phonon replica and 2LO phonon replica respectively. On the other hand, the luminescence from the C_{As} around 1.41 eV shows almost no change. This fact strongly suggests that Mn impurity at near the surface is increasing by H_2 ambient annealing so that the implanted Si-donor must be compensated by Mn_{Ga} acceptor. Furthermore, C_{As} accepter and other kinds of defect related recombination centers

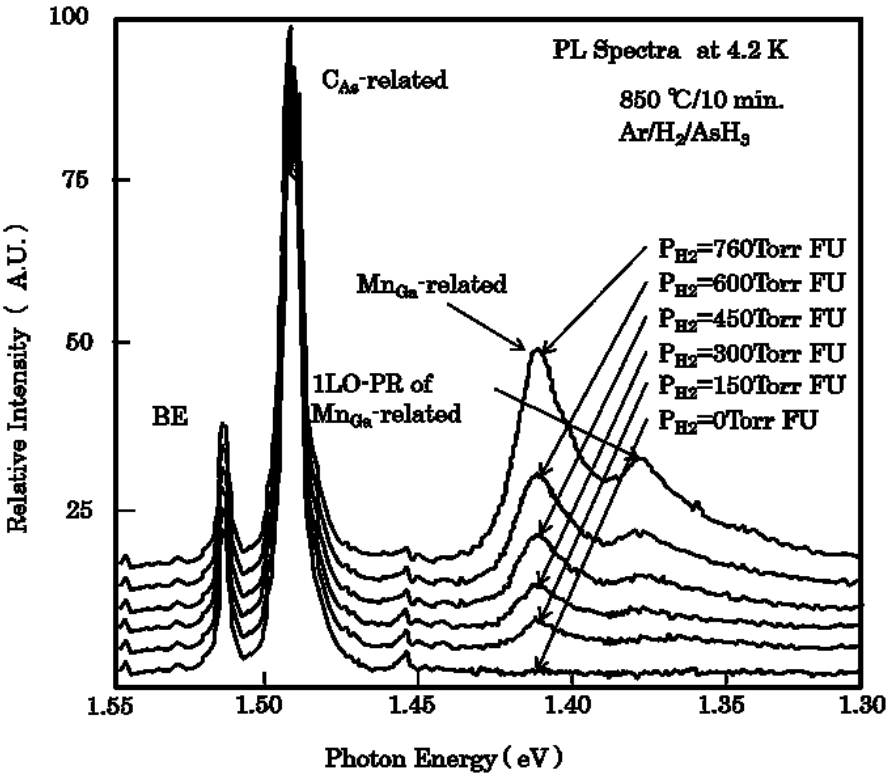

Figure 17: H_2 partial pressure dependency of photoluminescence spectra.

seem to have almost no contribution in the surface carrier loss. However, these photoluminescence studies are not quantitative but qualitative.

In order to clarify the quantitative estimation of the Mn acceptor contribution, direct observation of the Mn located near the surface is executed by using SIMS (SIMS: Secondary Ion Mass Spectroscopy) analysis. The depth profiles are easily obtained at the same time by using the sputtering. The SIMS apparatus is made of CAMECA corp., the model name is IMS-3F. The used first order ion source is O+ for the Mn distribution analysis. The standard samples made by Mn ion implantation are prepared to calibrate the results for the quantitative discussion.

The samples on the case with 0 Torr, 150 Torr and 450 Torr of H_2 partial pressure are analyzed and obtained Mn profiles are shown in Figure 18.

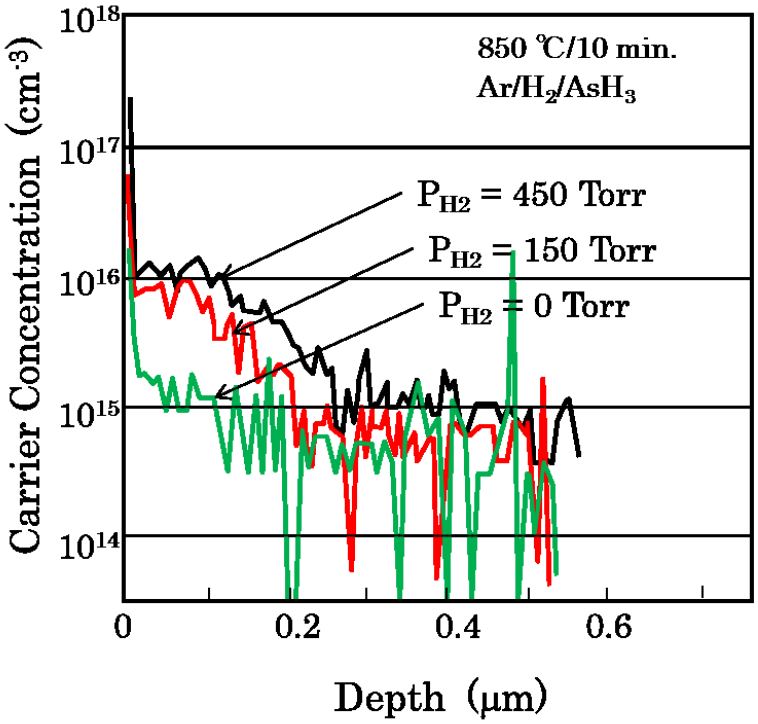

Figure 18: Mn depth profiles dependency on H_2 partial pressure at 850 ℃ / 10 minutes annealing measured by SIMS.

Although the X-axis inherently is a time scale which corresponds to the sputtering time it can be converted to depth scale easily by calculating the sputtering rate of O+ to the GaAs crystal. As for the Y-axis the relative intensity of detected ions is converted to concentration in the same way by virtue of the calibration using the Mn implanted standard sample. It is quite clear from the Figure 18 that Mn atoms are clearly piled up near the surface and it is increasing as the H_2 partial increasing.

The Mn is located in the depth range from the surface to 400nm and the peak concentration attains to the order of 2×10^{16} (atoms/cm^3) in the case of 450 Torr in H_2 partial pressure. This value is quite similar to the lost carrier estimated from the difference from the C-V profiles but it might be not completely explained only by the Mn accumulation. It is doubtless that Mn, which acts as an accepter, is sure to accumulate near the surface in the H_2 ambient annealing and it will be a main cause of carrier loss [23]. However, it is still unclear about the origin of the Mn and how it can be piled up at the surface. As far as the origin of the Mn is concerned, whether the kind of contamination from the experimental environment or the impurity essentially incorporated in GaAs substrate itself should be clarified. At the same time what is the motive force of the Mn piling up only in H_2 ambient must be revealed.

By careful observation of the difference between the C-V profiles in Ar based annealing and that of H_2 based annealing, the possibility of the etching in the GaAs surface is suggested. Therefore, whether the kind of etching happens or not in H_2 based annealing is investigated.

4.4 Etching phenomena

The samples used here are made by same conditions in Chapter 3.2, namely, samples are implanted with Si at the energy of 130 keV and a dose of 3×10^{12} cm^{-2}. Additionally, the samples without ion implantation are also prepared in order to confirm the affection of with or without implantation. Half of the sample surface is covered with Si_3N_4 film deposited by plasma CVD before annealing. Annealing is performed in a quartz tube in the temperature range from 850 to 925 °C exposing a

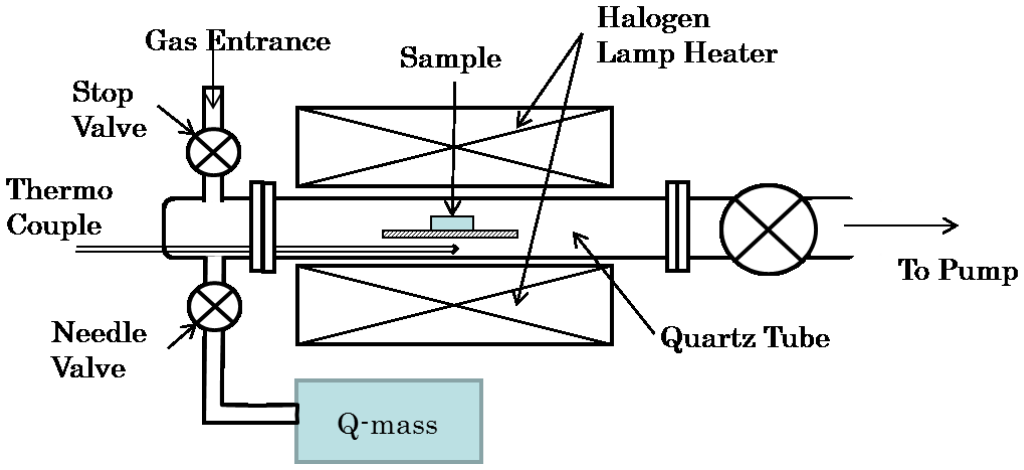

Figure 19: Schematic illustration for analysis of reacted gas by Q mass at 800 °C under the hydrogen pressure of 10 Torr.

sample surface to the gas flow in a FU configuration. A Taly-step is used to determine the etched depth after annealing in reference to the step between the region covered with Si_3N_4 and the uncovered region.

In another experiment samples are heated to 800 °C by a halogen lamp heater. Gaseous products produced by the reaction of GaAs with the ambient gas are sampled through another quartz tube branch and analyzed with a quadrupole mass spectrometer (Q mass) which is schematically illustrated in Figure 19.

Etched depths are plotted in Figure 20 after annealing at 900 °C under the H_2 partial pressure and AsH_3 partial pressure of 600 and 3 Torr, respectively. Open circles and open triangles represent the samples implanted with Si and not implanted, respectively. The two samples are etched essentially equally within experimental error. The etched depth increases linearly for the annealing time. The etching rate is 1.1 - 1.5 nm / min at 900 °C and P_{H2} : 600Torr. The etching rate did not depend on the flow rate of the mixture gas within the range from 0.825 to 3.3 l/min.

The temperature dependence of the etching rate is investigated in the temperature range from 850 to 925°C. The etching rate increases with increase of the annealing temperature under a constant partial pressure of H_2 and AsH_3, of 600 and 3 Torr, respectively. The Arrhenius plot of the etching rate shown in Figure 21 indicates the activation energy of 2.90 eV, which agrees well with the heat of

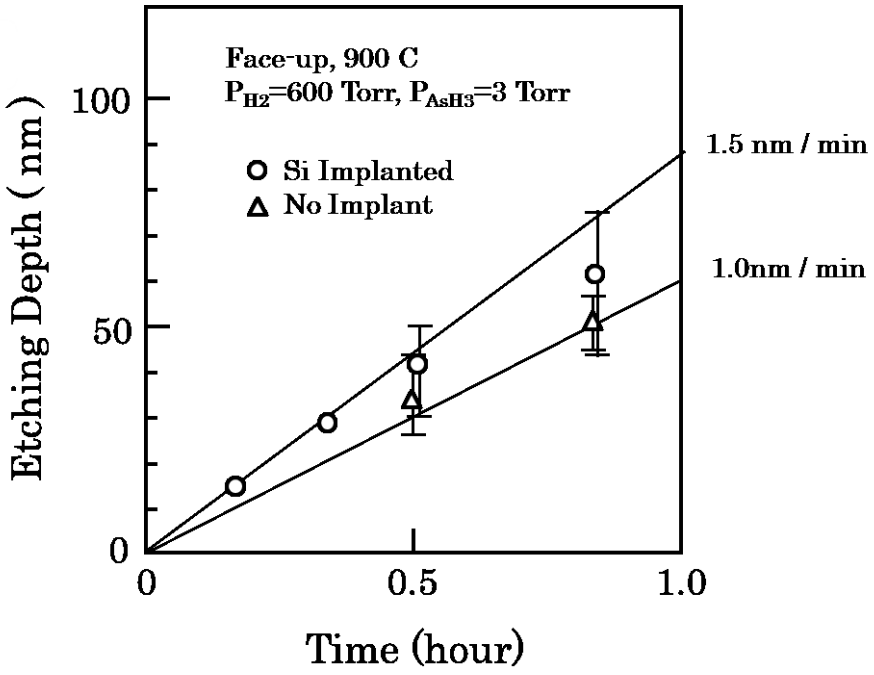

Figure 20: Etching depth vs annealing time at 900 °C under the hydrogen pressure of 600 Torr and arsine pressure of 3 Torr. Open circles indicate Si implanted samples and open triangles indicate not implanted samples.

evaporation of Ga [24]. It can be concluded that the thermal etching of GaAs in an H_2 ambient under excess arsenic pressure is governed by Ga evaporation [25].

The surface of the sample is smooth, and a mirror-like surface is preserved up to a temperature of 925 °C under excess arsenic pressure. It is indicating that Ga and As evaporated almost congruently by virtue of the suppression of desorption of volatile arsenic atoms under arsenic over pressure.

As described in Chapter 4.2, the Mn accumulation near the surface of GaAs is closely related to the partial pressure of H_2. Therefore, etching rate dependency of P_{H2} is quite important. The etching rate is plotted in Figure 22 as a function of P_{H2}, under the condition of a constant temperature of 900 °C and P_{AsH3} = 3 Torr. The etching rate increases with increasing P_{H2}. It is found that the etching rate is approximately proportional to the 3/2th power of P_{H2}. In fact, in Ar based annealing, which corresponds to H_2 based annealing of 0 Torr, there is no thermal etching at all.

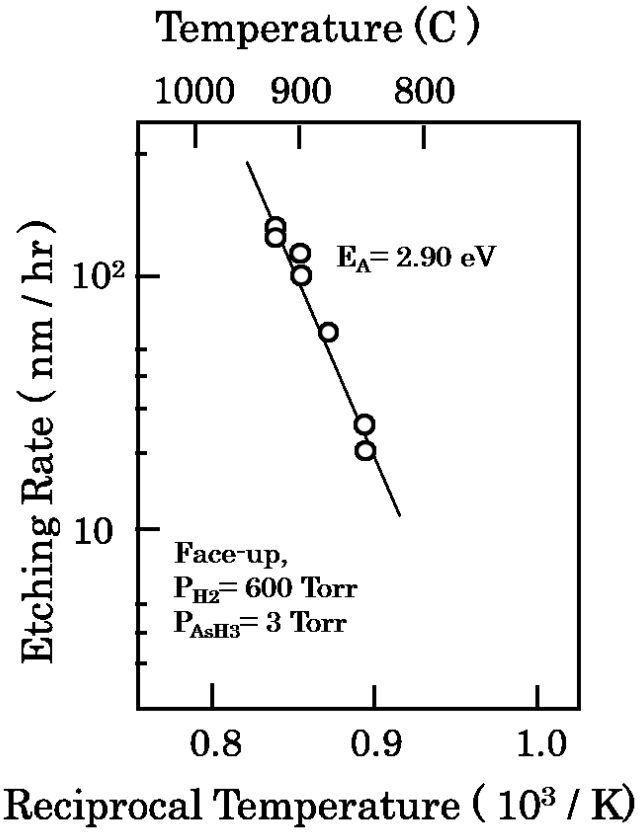

Figure 21: Arrhenius plot of the etching rate under the condition of P_{H2}=600 Torr and P_{AsH3}=3 Torr.

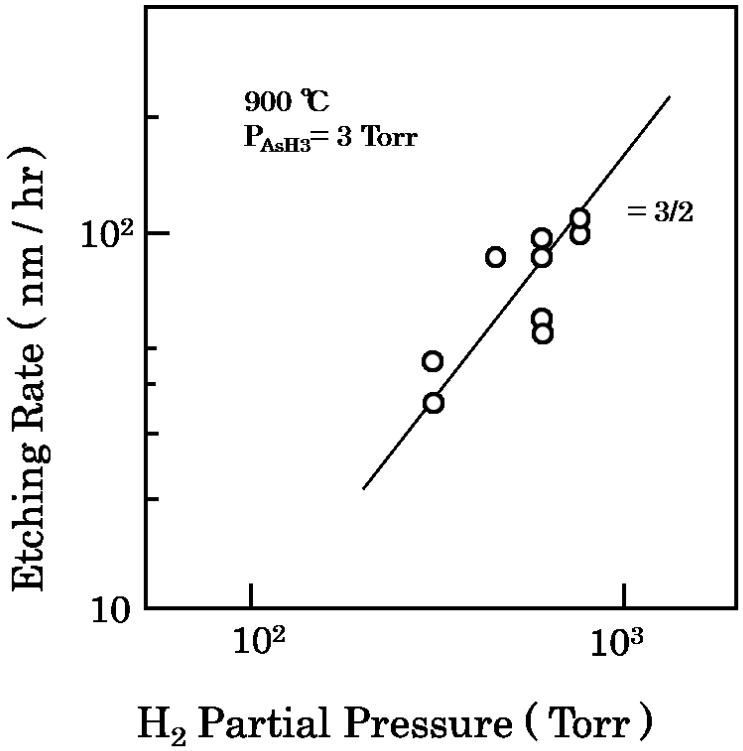

Figure 22: Etching rate as a function of hydrogen partial pressure at 900 ºC under the P_{AsH3}= 3 Torr.

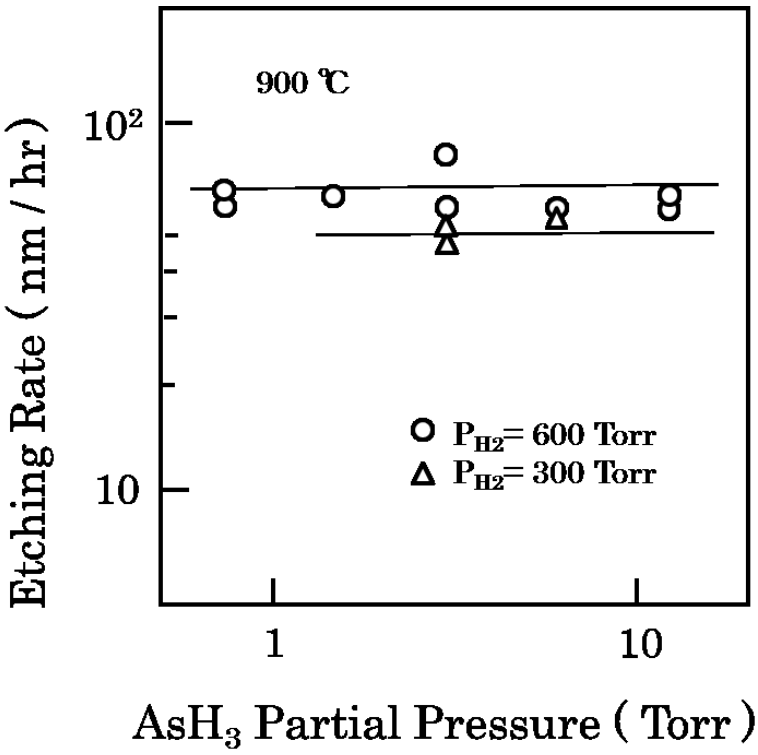

Figure 23: Etching rate dependence on AsH_3 partial pressure under the PH_2 of 600 Torr (○) and 300 Torr (△).

We also investigated whether varying the AsH_3 partial pressure would affect the etching rate. Annealing is performed at 900 °C under the conditions of P_{H2} = 600 and 300 Torr. The partial pressure of AsH_3 is varied from 0.75 to 12 Torr. No significant change in the etching rate is, however, observed either with P_{H2} = 600 or 300 Torr as is shown in Figure 23.

Gaseous species in a quartz reaction tube, during heat treatment of GaAs in H_2 or Ar ambient, are directly analyzed by the quadrupole mass spectrometer. No AsH_3 is introduced in this experiment. Figure 24 is a typical mass analysis spectrum obtained during heat treatment in the H_2 ambient, from which background spectrum is subtracted.

Arsenic (As+:75 amu), AsH family (AsH^+:76 amu, AsH_2^+:77 amu, AsH_3:78 amu) and As_2^+(150 amu) are observed in the spectrum. The arsine family must be due to an ionization process in the Q mass. On the other hand, no peaks are observed during heat treatment in the Ar ambient. There must be direct reaction of H_2 with

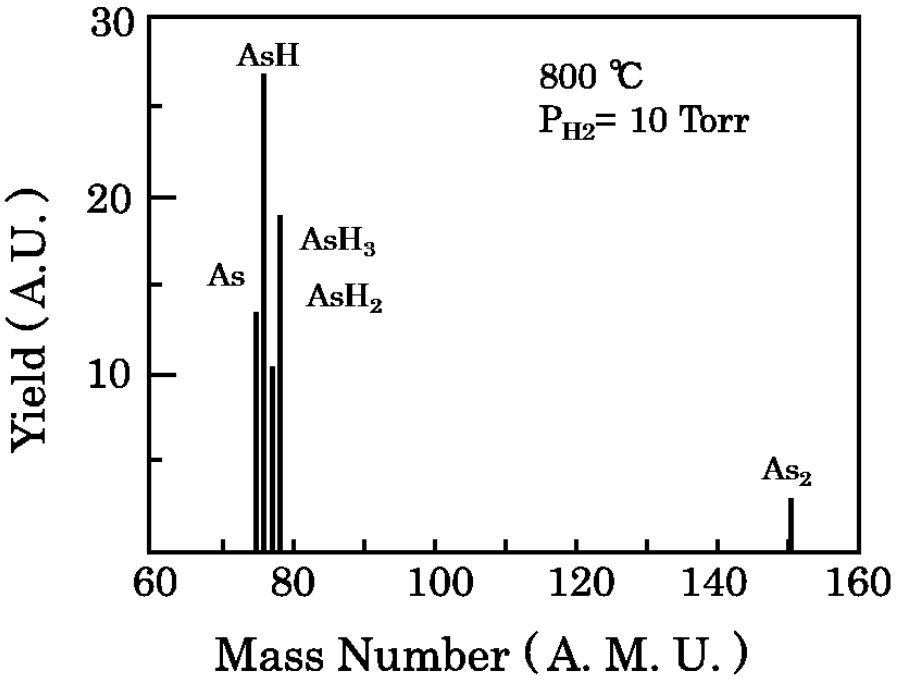

Figure 24: A mass spectrum of reacted gas during annealing in a 10 Torr hydrogen ambient at 800 °C.

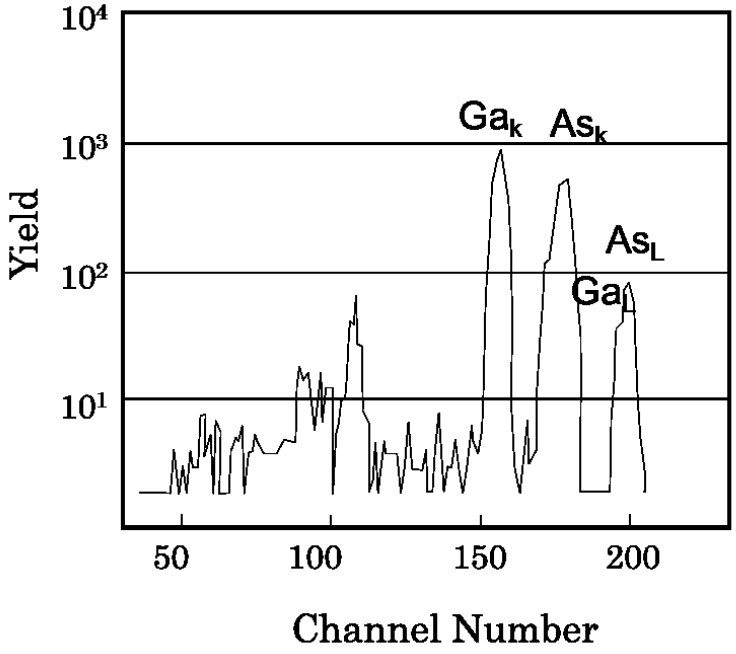

Figure 25: PIXE spectrum in the wall of quartz near the sample.

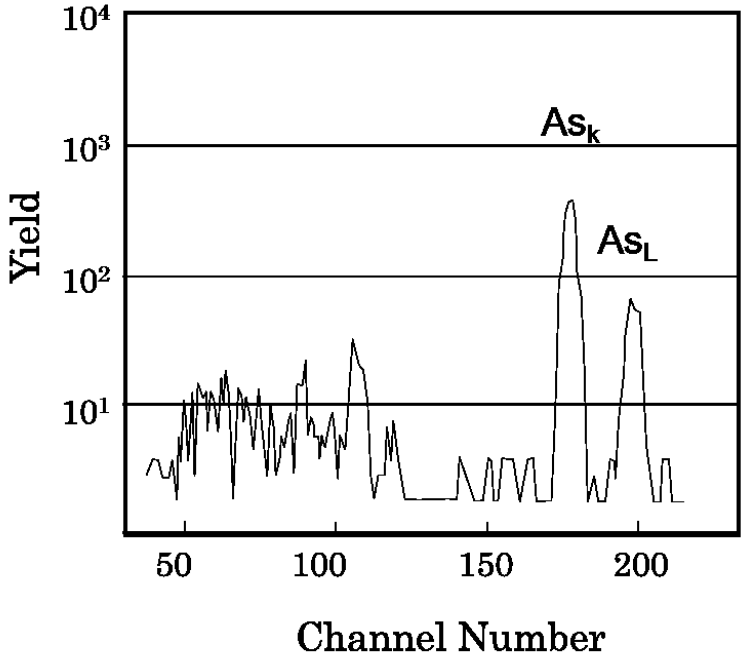

Figure 26: PIXE spectrum in the wall of quartz far from the sample.

GaAs at high temperature and must be a gaseous product. No Ga-related peaks are observed during heat treatment both in the H_2 and Ar ambient. Ga atoms are, however, detected on the wall of the quartz tube by an analysis using PIXE after the heat treatment in both of the ambient. However, detected Ga signal in Ar ambient is much lower than that in H_2 ambient annealing. Furthermore, Ga is only detected in

the wall of quarts tube near the sample. This fact can be explained by the low vapor pressure of Ga so that the evaporated Ga abruptly quenched and is deposited in the cold wall near the sample. These results are shown in Figure 25 and Figure 26. These experiments are executed by detecting the characteristic x-ray emission from the Ga atoms although the basics about PIXE analysis will be explained in Chapter 6.1.

4.5 Discussion about etching mechanism

Generally, dissociation of GaAs at high temperature is governed by the reaction and expressed by

$$GaAs \rightarrow Ga_{(s)} + 1/2\, As_2 \qquad (4)$$

or

$$GaAs \rightarrow Ga_{(s)} + 1/4\, As_4 \qquad (5)$$

Reaction (4) is dominant in the temperature range used in our experiments [26].

After annealing above 800 °C, thermal pits usually appeared at the surface of GaAs, leaving Ga droplets within the pits. No thermal pits are, however, observed in our experiment under arsenic overpressure. The surface of the sample thermally etches in H_2/AsH_3 ambient is smooth, mirror-like and free from crystallographic defects, suggesting congruent evaporation.

The temperature at which congruent evaporation occurs is determined using Eq. (4) or (5) as 637 °C by Arthur [27], 660 °C by Thurmond [24] and 625 °C by Foxon et. al [28]. These temperatures are much lower than the lowest temperature in our experiments. Eq. (4) or (5) is unlikely to dominate dissociation of GaAs under arsenic overpressure. The AsH_3 flow, which is considered to decompose most perfectly into H_2 and As_2 at our experimental temperature [24], gives an As overpressure of 3 Torr. This As overpressure corresponds to about 2 orders of magnitude higher than the As dissociation pressure of 1.5×10^{-2} Torr of GaAs at 900 °C [27]. The fact that the annealing under the Ar/AsH_3 ambient reveals no etching means the As dissociation process, Eq. (4) or (5), is well suppressed by As overpressure. The smooth and featureless surface after annealing at temperatures above 800 °C also must be due to the As overpressure.

Based on our experimental findings that the activation energy for thermal etch agrees well with the heat of evaporation of Ga, that the rate of thermal etch is proportional to the partial pressure of H_2 to the 3/2th power and that AsH_3 is detected in the reaction tube during annealing, we propose as the etching mechanism the chemical reaction (6),

$$GaAs + 3/2H_2 \rightarrow Ga(s) + AsH_3. \qquad (6)$$

This reaction is likely to occur because the bonding energy between H and As [29] is higher than that between Ga and As [30], AsH_3 [31] and PH_3 [32]. These bonding energy previously has been reported in the process of the reaction between atomic H and GaAs or InP at an elevated temperature. The pressure of AsH_3 to be expected by reaction (6) can be roughly estimated by the law of mass action and the quantity of As lost estimated by the etching depth. The estimated partial pressure of AsH_3 is as low as 1.3×10^{-8} Torr, which means that the estimated partial pressure of atomic H required for the reaction with GaAs is as low as 4×10^{-8} Torr. Fundamental chemical data says that more than 1×10^{-5} part of molecular H_2 decomposes to atomic H at the temperature considered [34]. It is strongly suggested that the kinetics involve the chemisorption of atomic H, as the first step, with subsequent reaction of H with As.

The law of mass action also tells us that the etching rate should depend on P_{AsH3}, which is inconsistent with our finding that the rate of thermal etching is independent of the partial pressure of AsH_3. This inconsistency is, however, resolved by the following reaction:

$$AsH_3 \leftrightarrow 1/2\ As_2 + 3/2H_2 \qquad (7)$$

Decomposition of AsH_3, that is, the reaction rate from the left to the right, is much faster than the reaction rate from the right to the left at the temperature considered [26]. AsH_3 introduced into the reactor must be decomposed into As_2 and H_2 by reaction (7). The partial pressure of As_2 does not directly affect reaction (6), that is, the rate of thermal etching independent of P_{AsH3}. AsH_3 produced by reaction (6) also must be decomposed immediately after the reaction. Reaction (6) is the intermediate reaction, leading to the decomposition of GaAs into Ga and As_2. A

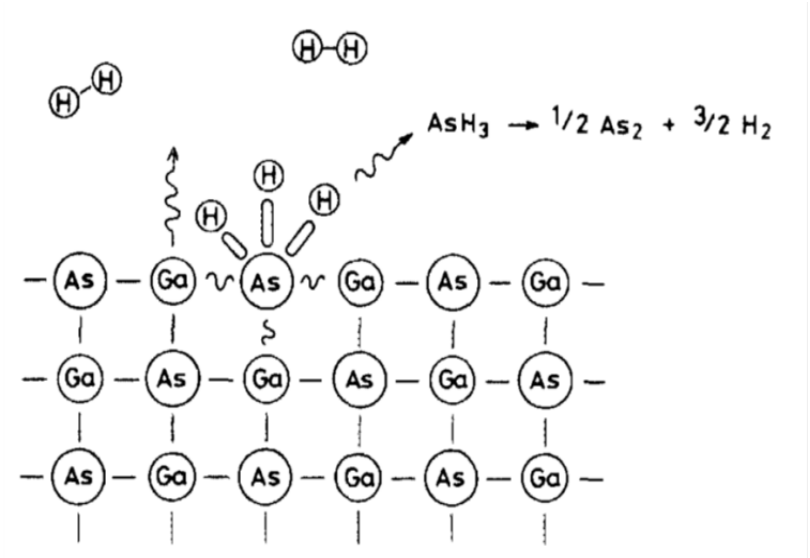

Figure 27: A schematic model for the thermal etching of GaAs with H_2.

mechanism for the thermal etch of GaAs with H_2 is proposed in Figure 27. The difference in the characteristics after high-temperature annealing in the H_2 ambient and the Ar ambient can be explained by the thermal etch.

GaAs surface is found to be etched by hydrogen above 800 °C. It is directly confirmed by a step which occurred after annealing at the boundary between the uncovered and covered region. The surface of the annealed GaAs is smooth, mirrorlike, and featureless when the thermal etching proceeded under arsenic overpressure, indicating that evaporation of Ga and As atoms take place congruently. The etching activation energy showed that thermal etching is governed by rate of Ga evaporation. The thermal etching is proportional to 3/2th power of P_{H2}. AsH_3 is detected by Q-mass analysis of the gaseous products during annealing. Direct reaction of GaAs with hydrogen is confirmed by these experimental facts [34].

Although the etching is taken place in H_2 ambient and the etching mechanism is revealed, the origin of the Mn is still unclear. As known well, the raw material of GaAs crystal is extracted from the residual of copper mine. GaAs is a by-product of copper and the impurities, like a Mn, Cu is included at an order of 10^{13} – 10^{14} atoms/cm^3. Therefore, it is quite natural that Mn is coming from the substrate itself and piling up in the surface during annealing. Actually a photoluminescence peak of 1.31 eV is also observed. As shown in the Figure 28, origin of this peak is thought to be Cu related one, furthermore, the intensity is largely dependent with the GaAs wafer providing makers. In the Figure 28, spectra of the substrate provided by maker "A" shows the peak of 1.31 eV, however, it is not clear in the that of provided maker B. This strongly supports the same piling up mechanism in deep acceptors of Ga site. If this hypothesis is right same phenomena will happen in un-doped semi-insulating GaAs substrate.

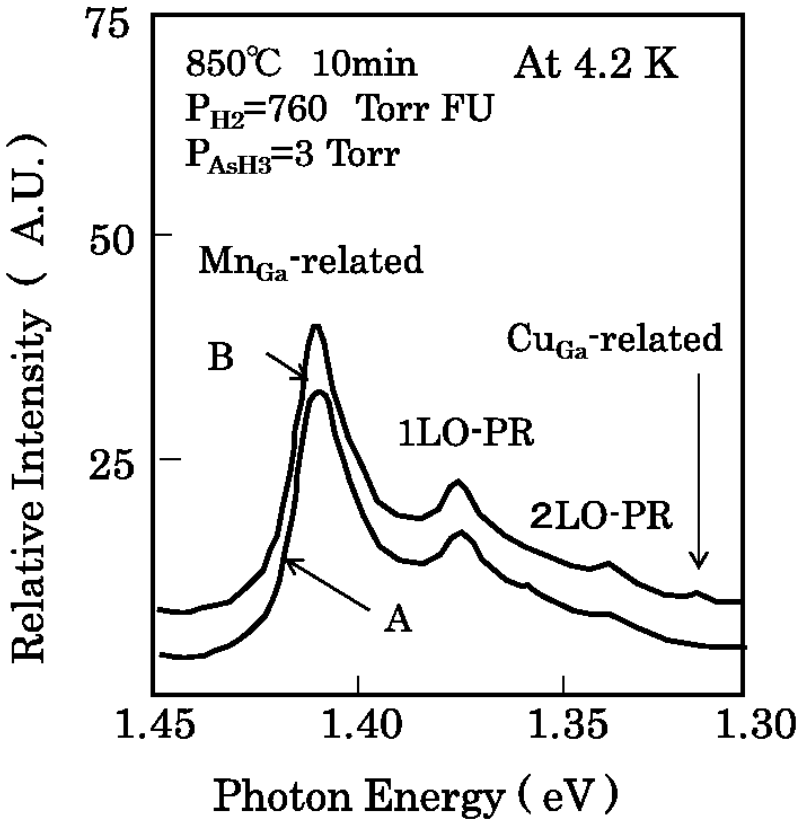

Figure 28: Wafer provider dependency of photoluminescence spectra near 1.3 - 1.45 eV.

Chapter 5

Thermal conversion in un-doped GaAs

5.1 Electrical properties in thermally treated un-doped GaAs

Conductive type conversion is sometimes reported in semi-insulating GaAs substrate after the high temperature annealing. These are, for instance, the n-type conversion in Cr-doped semi-insulating HB grown GaAs [11, 35] and p-type conversion in un-doped LEC grown GaAs [36, 37]. In the former case, a semi-insulating property is brought about by compensating the Si donor which is coming from the silica boat in the HB method growth with the Cr acceptor intentionally doped. N-type conversion after annealing above 800 °C in this case is interpreted that the balance of N_d(Si)-N_a(Cr) is collapsed by the out-diffusion of Cr during the high temperature annealing. In the latter case, namely in LEC grown GaAs, semi-insulating property consists of the balance with C_{As} acceptors and the EL2 donor derives from excess As. Therefore, p-type conversion in high temperature is said to be a result of out-diffusion of excess As.

Thus the thermal conversion is complicatedly depending on the nature of the semi-insulating. It is very important to know how the semi-insulating property is obtained and what kind of impurities contains. In this paper un-doped LEC grown GaAs is used and Mn pile up is observed in the Si-implanted samples only under H_2 ambient annealing. The samples are prepared for the thermal conversion experiments from the same lot of un-doped GaAs used in Chapter 3 and 4. The anneal experiments are performed in both Ar and H_2 ambient and in the temperature of 800 °C and 900 °C.

Table 4: Sheet carrier concentration of thermally converted samples versus atomic concentration of Mn calculated from SIMS.

Carrier Gas	Set-up	P_{AsH3} (Torr)	Temp. (°C)	Ns ($\times 10^{12}$ cm^{-2})	Mn ($\times 10^{12}$ cm^{-2})
H_2	FU	-	800	1.6	0.54
H_2	FU	3	900	1.4	2.3
Ar	FU	-	800	no conversion	0.04
Ar	FU	3	900	0.15	0.13

All the annealing time is 15min and 3 Torr partial pressure by AsH_3 is applied in the case of 900 °C to avoid dissolution of As. The evaluated results by Van Der Paw method is summarized in Table 4. All the samples show p-type conversion excepting the samples annealed in Ar ambient at 800 °C. The extent of p-type conversion is apparently proportional to the annealing temperature and the P_{H2}. The weak conversion in Ar /AsH_3 ambient at 900 °C is considered to be due to H_2 induced by dissolution of AsH_3. The results of the thermal conversion also support that annealing in H_2 ambient closely related to the formation of p-type carrier.

5.2 SIMS analysis in thermally converted samples

Mn distribution analysis is performed same as Chapter 4 using SIMS analysis method. The measured results are shown in Figure 29 and Figure 30 in the case of 800 °C and 900 °C annealing respectively. In both figures the dashed line is a result of no annealed samples. It is quite clear that the Mn piles up also near in the surface and that the extent of pile up is getting larger as the temperature and the H_2 partial pressure increasing. In order to confirm the quantitative contribution of Mn concentration to the p-type concentration, the sheet concentration of Mn piled up is calculated by the integration of Mn in Figure 29 and 30. The results are shown in Table 4 too. The sheet carrier concentration of p-type is well accordance with Mn sheet concentration in the case of 900 °C annealing. However, in the 800 °C /H_2 annealing, that of p-type is 3 times larger compare to the Mn sheet concentration. It is slightly curious results and implies that there would be other factor not to be perfectly grasped.

The Si distribution is also investigated in order to clarify the inconsistency in the Table 4 by using SIMS analysis too. For the detection of the Si, Cs^+ ion is used as a 1st order ion source. The results are shown in Figure 31 and 32 in the case of 800 °C and 900 °C respectively. The results are marvelous because a lot of Si atoms are accumulated simultaneously near the surface both in the case of 800 °C and 900 °C annealing. Especially, the concentration of Si attains in the vicinity of 10^{18} cm^{-3} with the case of 800 °C / H_2 annealing as is shown in Figure 31. The Si concentration attains order of 4×10^{17} cm^{-3} even in the case of 800 °C / Ar as is shown in Figure 31 too. The concentration of Si in the case of 900 °C is also high as is shown in Figure 32 although the level of accumulation is lower than the case of 800 °C. This may come from the effect of the As over pressure. Almost the detected Si must be not in the site of Ga because all the samples show p-type. The possibility of the status of Si left is the case in As site or interstitial. The Si distribution in the Figure 31 and 32 indicates very fast diffusion coefficient if the Si is not coming from outer side but through the

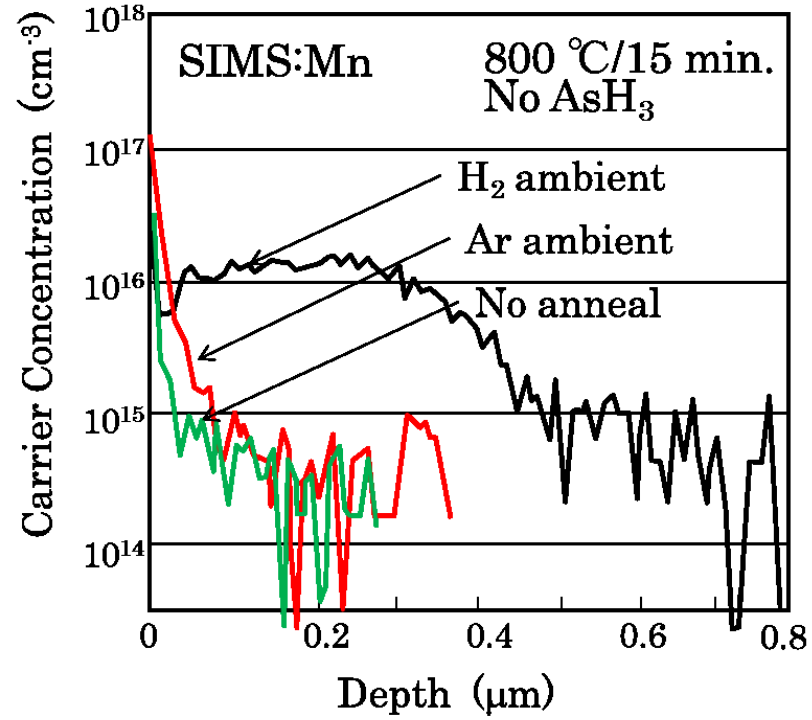

Figure 29: Mn depth profiles of un-doped GaAs measured by SIMS after 800 ℃ / 15 min annealing.

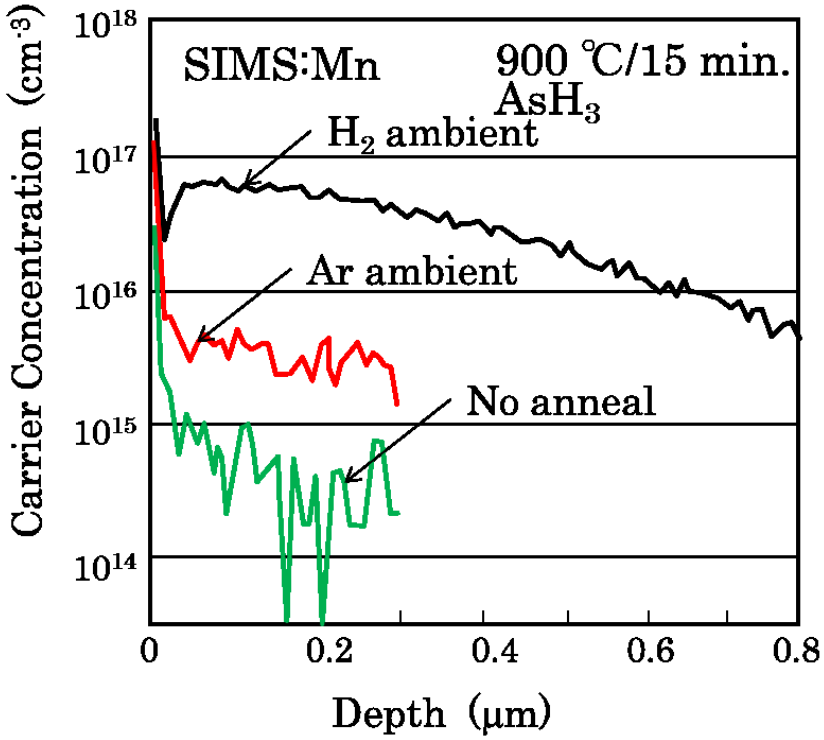

Figure 30: Mn depth profiles of un-doped GaAs measured by SIMS after 900 ℃ / 15 min annealing.

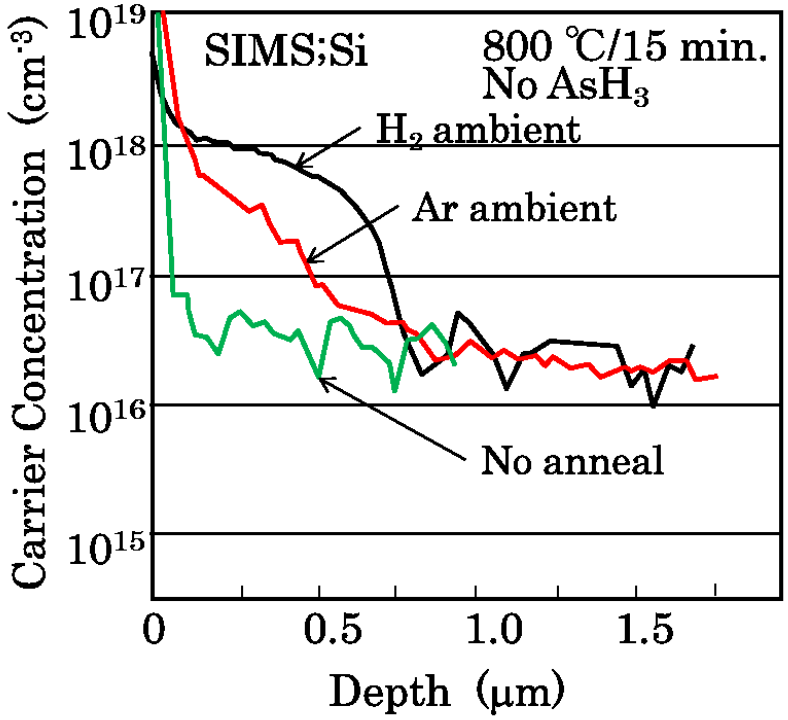

Figure 31: Si depth profiles of un-doped GaAs measured by SIMS after 800 ºC / 15 min annealing.

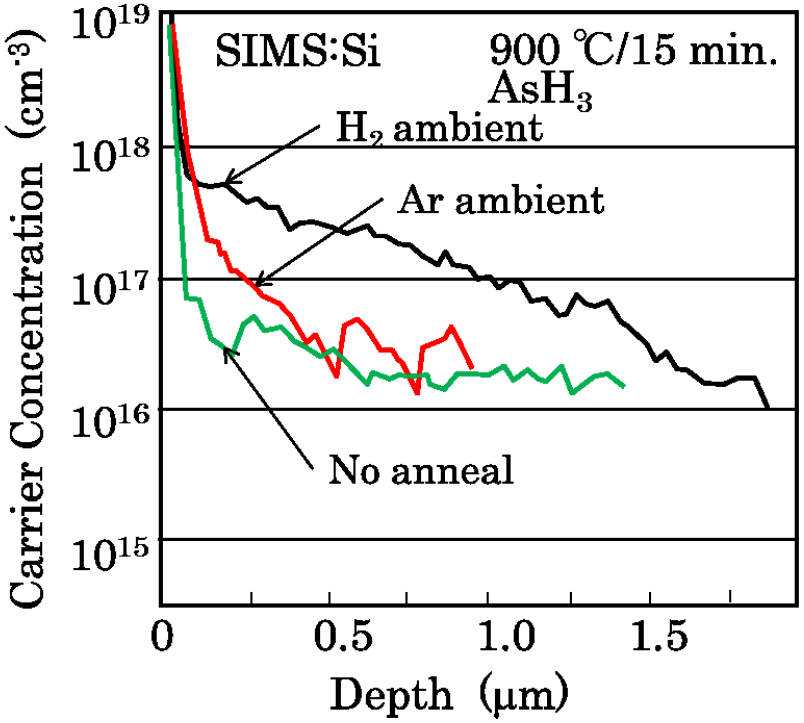

Figure 32: Si depth profiles of un-doped GaAs measured by SIMS after 900 ºC / 15 min annealing.

substrate. If almost the Si is in the interstitial site Si does not acts as both accepter and donor, furthermore, very fast diffusion constant is also well explained. At the same time the large Si accumulation in 800 °C annealing is explained by the increasing of Si_{As} acceptor because there is no As over pressure. This assumption is well in accordance with the result of 800 °C / H_2 in Table 4. Furthermore, we must pay attention to the fact that the profile of Si in Figure 31 and Figure 32 is very similar to that of Mn in Figure 29 and Figure 30. These facts suggest strongly that Si and Mn diffuse same way and affecting each other. One of the possibilities is making a kind of pair of Mn and Si because Mn_{Ga} acts as - charge and Si_{Ga} acts as + charge in the high temperature.

In order to clarify the accumulation mechanism of Mn it is useful to investigate the thermal properties of Si in GaAs. One of the important factors is to know the site position of Si in GaAs and how it is changed by the thermal treating. Regarding the site position of Si there are three possibilities, these are $Si_{Ga,}$ Si_{As} and interstitial. The studies using RBS/PIXE method is very effective to determine the site position of the dopant in Zincblende structure. In the next chapter the results of the site position evaluated by RBS/PIXE is described.

Chapter 6

Crystallographic studies by RBS/PIXE

6.1 Basis in RBS and PIXE analysis

In order to investigate the status of the implanted Si RBS/PIXE analysis is employed. RBS (Rutherford backscattering spectroscopy) is well known as an analysis method which can evaluate the crystallography. It can estimate quantitative atomic density by analyzing the energy distribution of the back scattered probe atoms. Normally, He^+ or H^+ are used as probing ions and this probing ion have an energy information of target atoms because the backscattering can be considered as a results of perfect elastic collision. The limit of detection is about an order of 10^{18} cm^{-3} and it is relatively lower sensitivity because the probability of the complete elastic collision is extremely low. On the other hand, PIXE (particle-induced x-ray emission) can analyze the species of target atoms by analyzing the energy of characteristic x-ray emission. Furthermore, we can analyze the crystallography or identify the position of dopant by utilizing the asymmetry of the crystal and the channeling effect. All the experiments in this Chapter are performed under the collaboration with research laboratory have a Van de Graaff accelerator in Hokkaido University. The samples prepared here are (100) oriented un-doped LEC grown GaAs too. The Si ion implantation performed with the energy

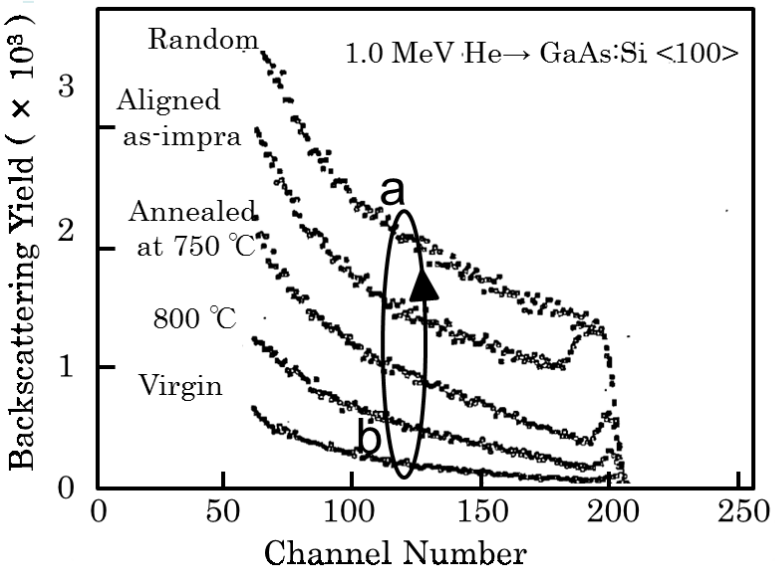

Figure 33: Typical RBS spectrum versus annealing temperature.

of 100 keV and the dose is varied with the range of 1×10^{15} to 1×10^{16}. Annealing at 750 °C, 850 °C, 900 °C and 10 minutes is performed in $H_2/Ar/AsH_3$ ambient with FF configuration.

The typical RBS spectra are shown in Figure 33 with the He^+ probe ion accelerated in 1.0 MeV. The Y-axis expresses the intensity of back scattered probing atoms. The X-axis indicates the energy of back scattered ions and it is including the depth information and atomic number of target atoms. It is quite difficult to separate the signals clearly from Ga, As and Si in the RBS spectrum because the each atomic number is very near. On the contrary, it is very easy to separate each signals in the PIXE analysis as is shown in Figure 34. A x-ray emission energy of each atoms has unique value so that we can dissociate the target signal from other signals. Figure 33 shows typical characteristic x-rays spectra of Si-implanted GaAs measuring the orientation of <100> axis. 1.00 MeV accelerated H^+ ions and a Si(Li) p-i-n detector are used for the PIXE analysis. The ion beam diameter and its divergence were 1.0 mmϕ and 0.03", respectively.

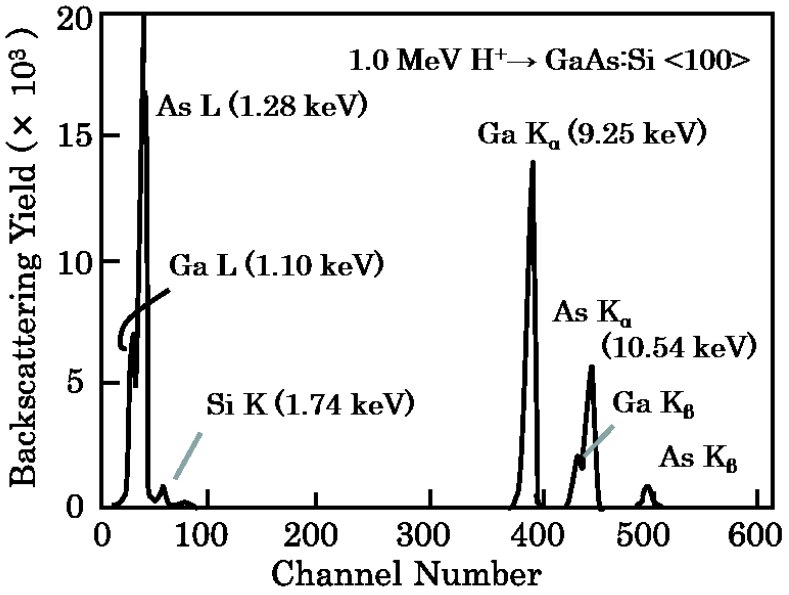

Figure 34: Typical PIXE spectrum for Si implanted GaAs.

As shown in Figure 34, the characteristic x-ray peaks from the each atoms is explicitly recognized and they are clearly split. This implies measurement of the light atoms in heavy host crystal like as Si in GaAs is possible. It is one of the advantages as using ion beam probes that crystallographic analysis is possible both in RBS and PIXE measurement. The scattering field along random direction as is shown in Figure 33 is very high by the de-channeling effect. On the contrary, the scattering yield along the specific direction is very low by the channeling effect. If the scattering yield along the specific axis direction is high the sample has some

disorder from the crystallographic view. Figure 32 shows the process of the recover in the crystallography of GaAs by the annealing after the ion implantation. If the probe beam is rotated around the some crystal axis to the de-channeling direction the measured yield changes continuously like as shape of valley. For instance, the yield change which is obtained by scanning the beam between <100> axis aligned direction (point (a) in Figure 33) to random direction (point (b) in Figure 33) is shows in Figure 35. The depth of the bottom in Figure 35 means the crystallographic goodness. We can define the figure of merit by using the ratio of the yield in channeling direction to that in random direction. This is called χ_{min} , namely,

$$\chi_{min} = \chi_{channeling} / \chi_{random} \quad (8)$$

If χ_{min} shows near 1 it means the sample is no more than the crystal but amorphous state from the view point of ion channeling. Here, we must notice the limit of analytical depth. It is estimated about an order of 100nm in our case when the H^+ ion probe is used and its energy is around 1MeV and also the distribution in the depth cannot be revealed. These features are basically same in PIXE analysis [38].

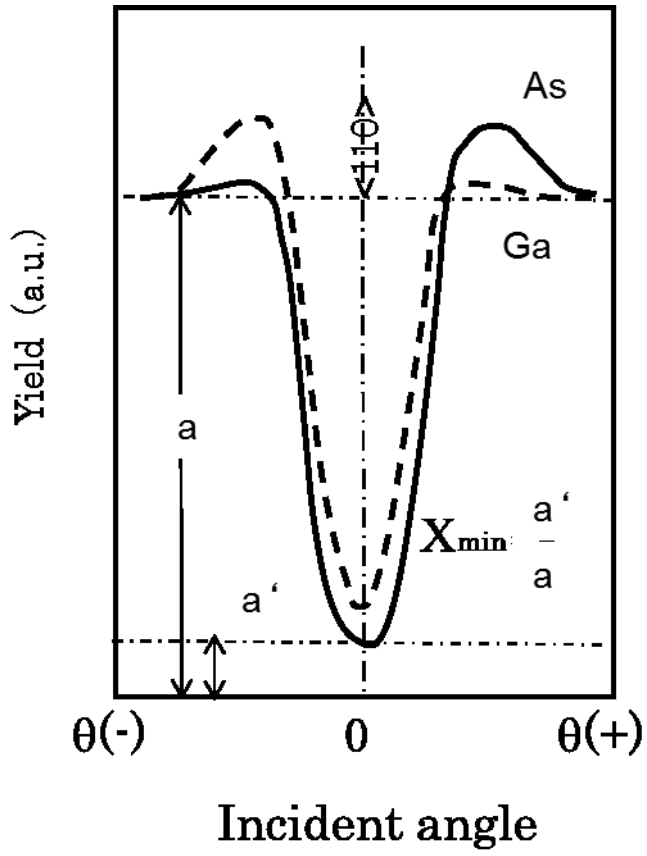

Figure 35: Asymmetric X-ray yield around <100> axis.

Furthermore, site position of impurities in host crystal can be determined by using analysis along the specific direction and by combining RBS with PIXE

analysis. In the zinc-blend structure like a GaAs crystal the asymmetry structure along the <110> axis can be used for this analysis [39, 40]. The atomic arrangement in (110) surface of GaAs is shown in Figure 36. The Ga strings and As strings are alternately arranged along the <110> direction. The As strings will be masked with the Ga strings when the incident angle of the probing beam inclined to the direction of $\theta^{(+)}$. In consequence, the signal is mainly coming from the atoms in the Ga strings. If the dopant of the Si occupies Ga site the characteristic x-ray from Si_{Ga} will be detected. On the contrary, Si_{As} (Si in As site) can be detected by tilting the probing beam for the direction of $\theta^{(-)}$. Thus, it is possible that the site of dopant Si is determined by using the asymmetrical nature of the crystal. The properties of Si dopant in the process of annealing after ion implantation is investigated and it will be described in the next Chapter 6.3.

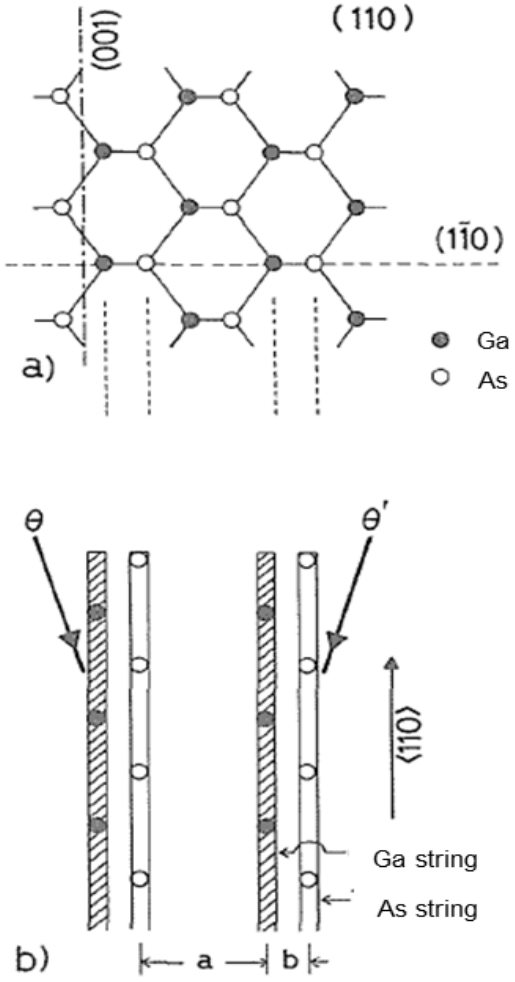

Figure 36:
a) Arrangement of Ga and As in the normal plane to the <100> direction.
b)Distribution of Ga and As atomic strings in the (110) plane. θ and θ' indicate the incident directions of ions.

6.2 Properties of Si dopant in annealing process

As described at Chapter 4 and Chapter 5, Mn pile-up near the surface is responsible for carrier loss of Si implanted GaAs in high temperature annealing and p-type conversion in thermally annealed un-dope GaAs. In addition, it is found this phenomenon strongly is related to the etching of GaAs surface by H_2 ambient annealing. Almost the carrier loss in the surface is explained quantitatively by the Mn_{Ga} acceptor piled up in the surface. However, Si pile up is also observed in thermally p-type converted GaAs. Since the Si dopant is an amphoteric element toward GaAs, namely Si_{Ga} acts a donor and Si_{As} acts as an acceptor, the thermal properties of Si_{Ga}, Si_{As} and its ratio must be clarified. Furthermore, although it is said that self-compensation mechanism is main cause of carrier saturation in highly Si implanted GaAs, there is no evidence so far. In this Chapter the quantitative properties of Si-site in GaAs crystal are investigated by the RBS/PIXE analysis

The GaAs samples are implanted by Si with the energy of 100 keV and the dose range from 10^{12} to 10^{16} cm^{-2}. The annealing is performed typically at 850 °C in the ambient of $Ar/H_2/AsH_3$, here, the partial pressure of Ar, H_2, AsH_3 is 600 Torr, 150 Torr and 3 Torr, respectively. The annealing set up is FF method and annealing time is 10 minutes excepting the sample with the dose of 10^{16} cm^{-2}. The annealing time is varied in the range of 10, 30 and 60 minutes only for the samples in the dose of 10^{16} cm^{-2}.

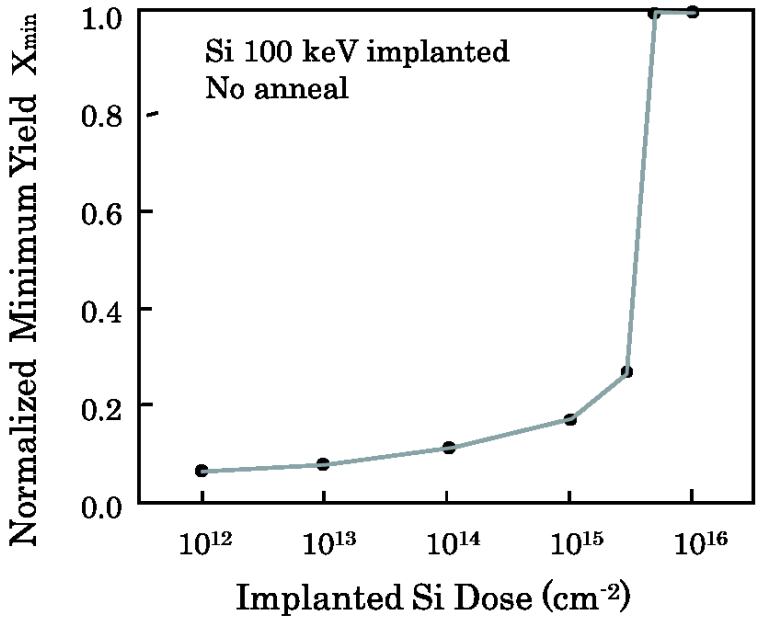

Figure 37: The normalized minimum yield ･min obtained by RBS analysis after Si implanted in the range from 10^{12} to 10^{16} cm^{-2}.

The normalized minimum yield χ_{min} is investigated by using RBS spectra with the samples which Si implanted in the range from 10^{12} to 10^{16} cm^{-2}. The results are shown in Figure 37 and it is found that GaAs keeps its crystal structure up to the Si dose of 3×10^{15} cm^{-2}. The crystallography suddenly degraded in dose of 5×10^{15} cm^{-2} and this means GaAs is to be almost amorphous state in this dose from the viewpoints of ion channeling.

The annealing temperature dependency of χ_{min} for Si and host atoms is investigated in the case with sample of $10^{16}cm^{-2}$ in order to look up the recovering process in the damaged layer. The results are shown in Figure 38 and it is found that the damaged layer of host atoms restored the crystallography gradually by increasing the annealing temperature. In addition, the recovering process in crystal viewpoints is saturated in 900 °C.

Generally, the lattice occupation ratio of impurities are expressed by

$$(1- \chi_{min\ (impurity)}) / (1- \chi_{min\ (host\ atoms)}) \qquad (9)$$

Here, $\chi_{min\ (impurity)}$ is a χ_{min} in impurities obtained by PIXE and $\chi_{min\ (host\ atoms)}$ is a χ_{min}

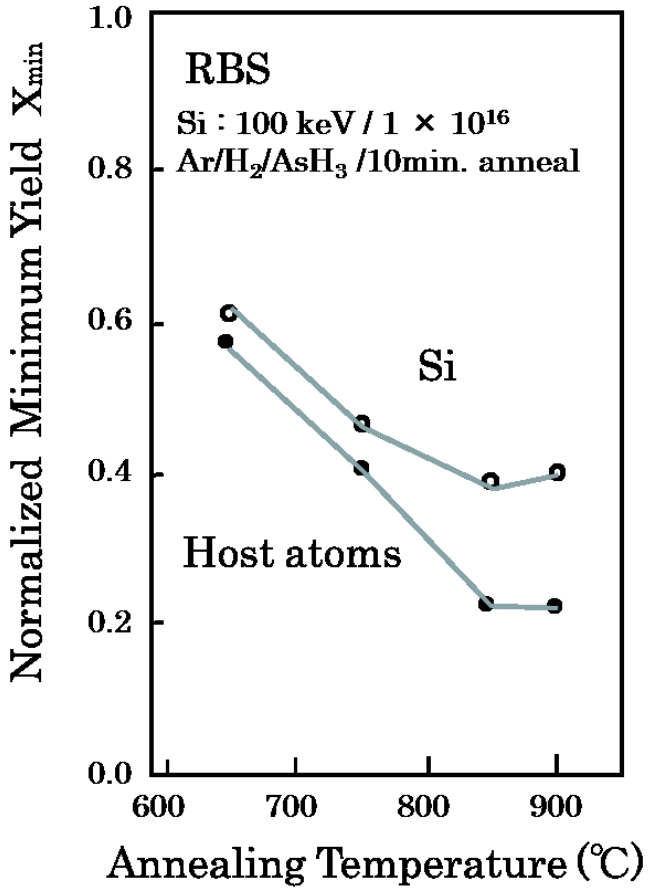

Figure 38: Annealing temperature dependency of χmin obtained by RBS with the sample at the dose of 10^{16} cm^{-2}.

in host atoms obtained by RBS. Based on this equation and using asymmetry along the <110> axis, we can easily calculate the each site occupation ration of Si in GaAs lattice site, namely Si_{Ga} and Si_{As}. The calculated χ_{min} of Si in Ga site and that of As are shown in Figure 39. The implanted Si occupies preferentially Ga lattice site and it is increasing as the temperature rising up to 850 °C. In addition, Si_{Ga} decreasing at 900 °C and Si_{As} have a tendency of moderate increasing. The lattice site occupation of Si_{Ga} and Si_{As} is 52 % and 13 %, respectively at 850 °C. Total site occupation ratio is about 65 % and this is slightly small value. The rest 35 % of Si atoms probably is in the distorted lattice position or interstitial position. Although this value is surprisingly large we should notice the dose of this experiment is much higher than usual and the crystal is getting to amorphous or heavily disordered state as implantation.

In order to investigate the dependency of the site occupation ratio on implantation dose, RBS/PIXE measurement are performed on the samples Si implanted in the range of $1 \times 10^{12} - 1 \times 10^{16}$ cm^{-2} before/after annealing at 850 °C

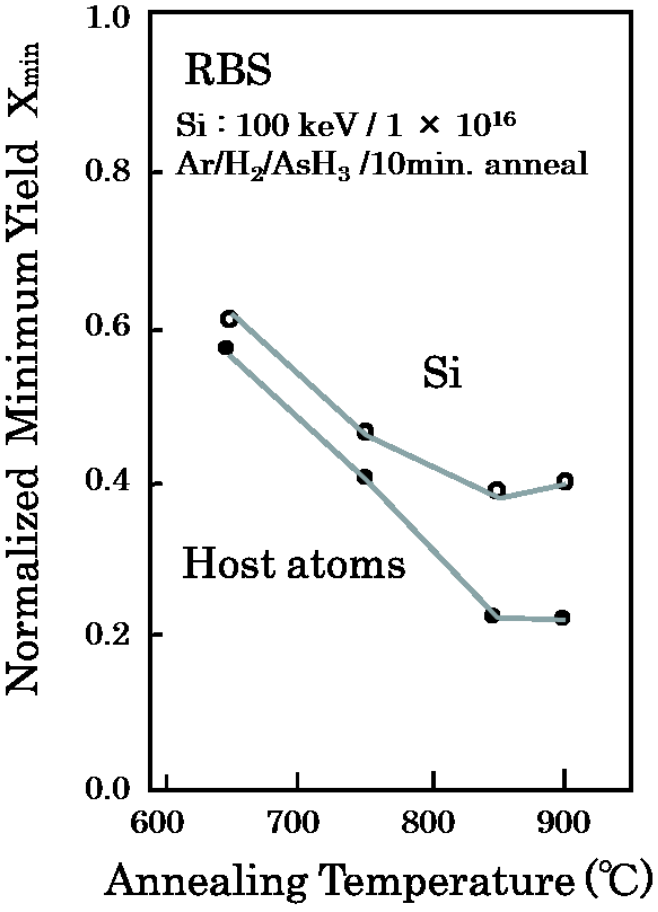

Figure 39: Annealing temperature dependency of χmin in Si_{As} and Si_{Ga} determined from PIXE measurement at the Si dose of 10^{16} cm^{-2}.

and 10 minutes. The results are shown in Figure 40 and it is easily understood the crystalline almost completely restored up to 7×10^{15} cm^{-2}. Furthermore the sample with dose of 1×10^{16} cm^{-2} still have a disorder after annealing. This change is so sensitive to the dose of Si atoms. The calculated each site occupation ratio of Si in the range of $1 \times 10^{15} - 1 \times 10^{16}$ cm^{-2} is shown in Figure 40. Each occupation ratio of

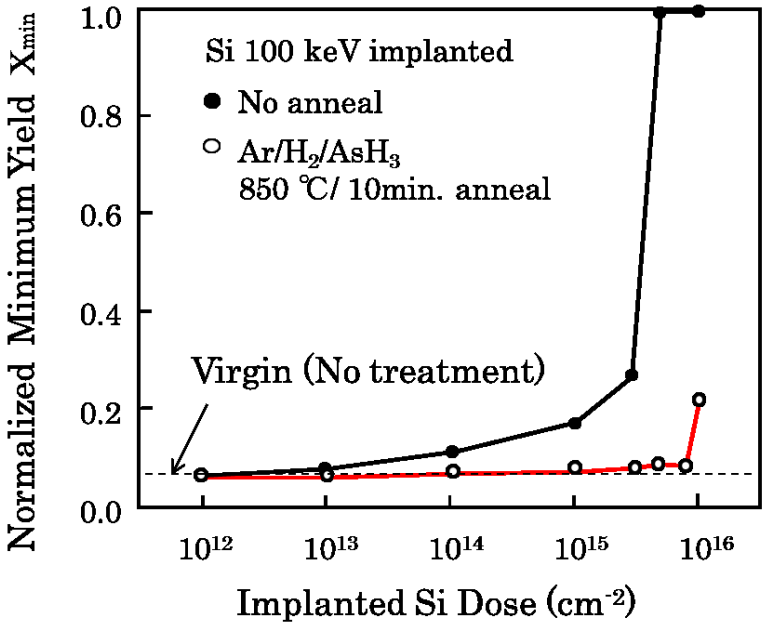

Figure 40: Si dose dependency of ･min obtained by RBS analysis after 850 ºC / 10 minutes annealing.

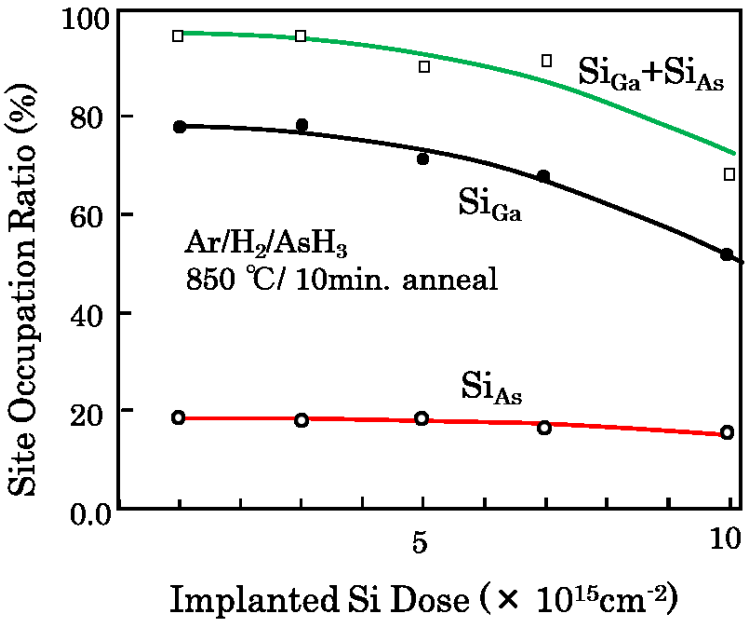

Figure 41: Si site occupation ratio in 1-10 $\times 10^{15}$ implanted sample after 850 ºC / 10 minutes annealing.

Si_{Ga} and Si_{As} is not so much changed in the range of $1 \times 10^{15} - 5 \times 10^{15}$ cm^{-2} and each ratio is almost 80 % in Si_{Ga} and 20% in Si_{As}. Calculated total site occupation ratio (Si_{Ga} + Si_{As}) is also shown in Figure 41. It is about order of 90 – 95 % and it gradually decreases to the dose of 5×10^{15} cm^{-2}. This value is quite acceptable and higher Si

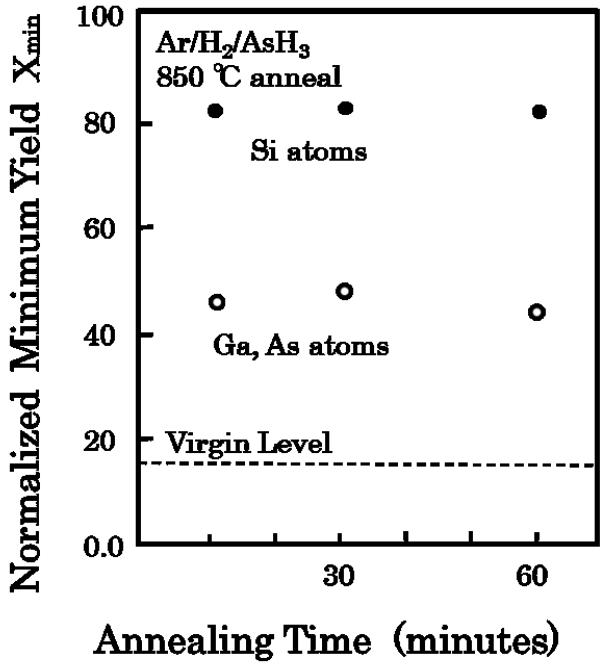

Figure 42: Obtained χmin of Si and host atoms (GaAs) by RBS .

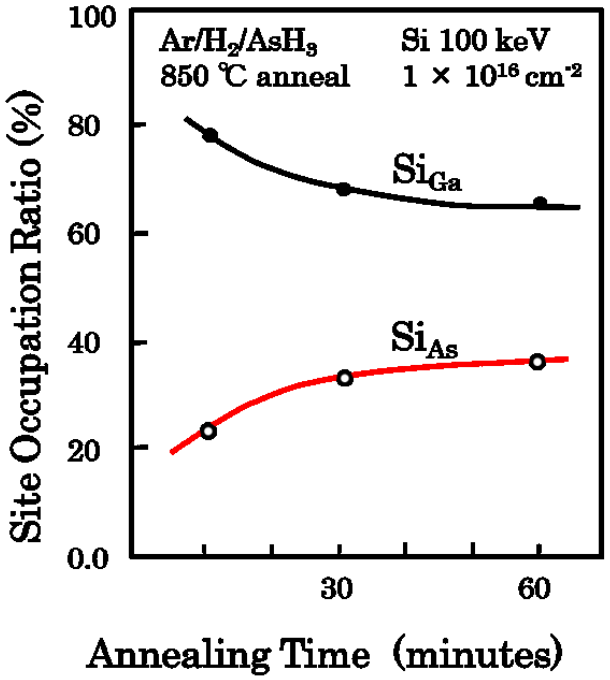

Figure 43: Anneal temperature dependency of Si site occupation ratio.

site occupation ratio over 95 % is conjectured analogically in lower dose of 1 – 5 × 10^{13}cm^{-2} normally used for the FETs. The occupation ratio suddenly drops to the 65 % in 1 × 10^{16} cm^{-2}. This results well coincides with that of Figure 40 and the results show that the crystalline of the sample with dose of 1 × 10^{16} cm^{-2} is not sufficiently restored by the annealing. As far as the annealing temperature is concerned 850 °C is a most appropriate as is described above. However, it is thought that the crystalline of the sample in dose of 1 × 10^{16}cm^{-2} still remain in the disordered state.

The annealing time dependency of crystalline in the heavily implanted GaAs is investigated. The annealing temperature is fixed at 850 °C and the annealing time is varied from 10 to 60 minutes. The samples with dose of 1 × 10^{16} cm^{-2} are used for this experiment. The obtained χ_{min} of Si_K by PIXE and host atoms (GaAs) by RBS are shown in Figure 42. It is found that the crystalline of these heavily implanted ratio of calculated from Figure 42 is shown in Figure 43. It is clear that the crystalline does not restore, nevertheless, gradually Si site transfer takes place as the annealing time increasing. This phenomenon is same as the case of 900 °C

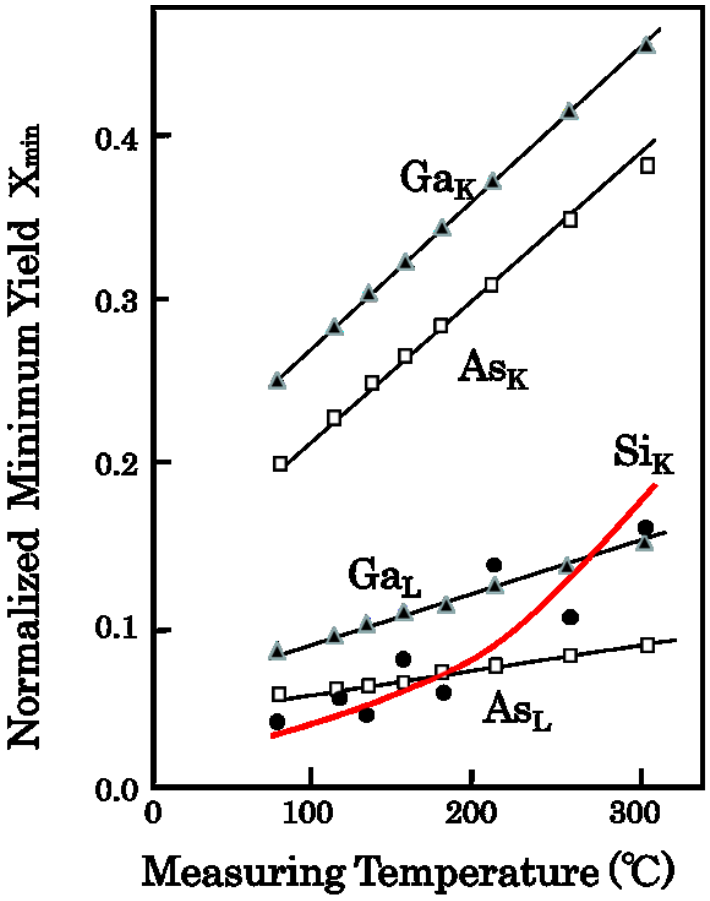

Figure 44: Measuring temperature dependency of χmin in characteristic x-ray from Si, Ga and As.

annealing so that some kinds of over annealing occurs and the Si site transfer takes place in spite of As over pressure is applied during annealing.

The temperature dependencies of χ_{min} of Si and host atoms by PIXE are investigated in order to clarify the state of the implanted Si in detail. All the annealing condition is 850 °C and 10 minutes. The obtained results are shown in Figure 44. Normally the slope of χ_{min} is thought to be linearly changed like a case of Ga and As shown as Figure 44 according to the model of Barrett [45]. However, χ_{min} of Si_K especially in $2 \times 10^{15}cm^{-2}$ is exponentially increasing as measuring temperature increasing. Furthermore extrapolated χ_{min} of dose of 2 x 10^{15}, 3 x 10^{15} and $7 \times 10^{15}cm^{-2}$ at 0 K is about 0.04, 0.10 and 0.18, respectively. These values are much larger than 0.03 which is expected value of the case with ideally distributed Si. This fact implies that the Si atoms are displaced from the inherent lattice site. This displacement of the dopant is observed in AlGaAs and it is well known it forms the some deep level acceptor with novel features [46]. Further investigation must be required to determine whether the observed displacement is same thing with the

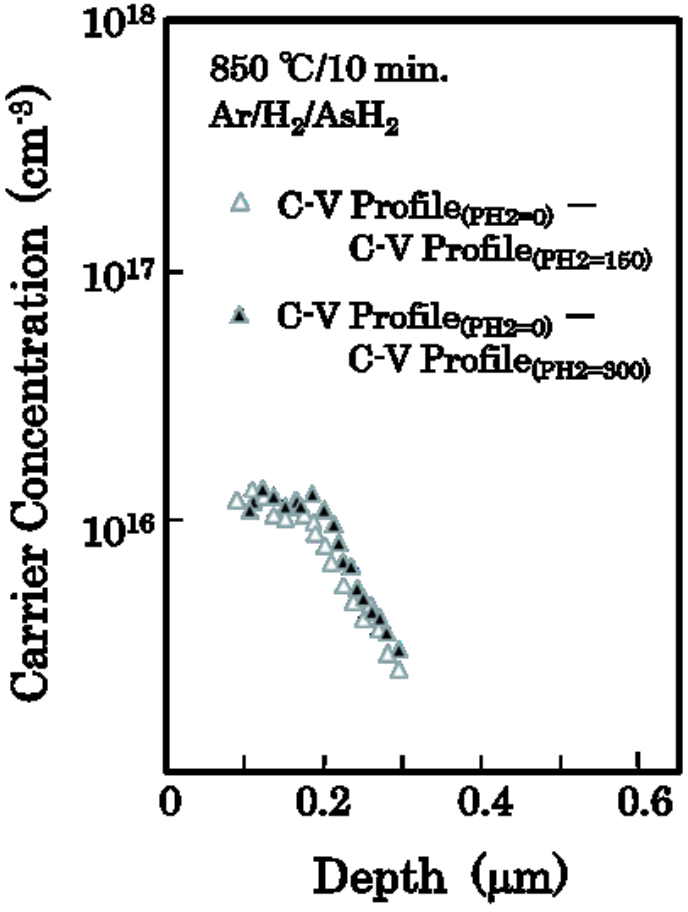

Figure 45: Re-calculated lost carrier distribution under the consideration of surface etching.

case of AlGaAs or not. However, it can be concluded that some kind of lattice distortion is more responsible for the carrier compensation mechanism in heavily Si implanted GaAs rather than the Si site transfer.

Thus the lattice site of the implanted Si is studied by RBS/PIXE [47]. The occupation ratio of Si_{Ga} and Si_{As} is estimated almost order of 80 % and 20 % respectively. Furthermore, the Si dopant occupies almost lattice position. It is thought to be same within the experiment condition in Chapter 4 and Chapter 5.

Therefore, in the process of Mn out-diffusion described in Chapter 4 and Chapter 5 Si site transfer, namely self-compensation mechanism, probably has a no direct relationship with carrier loss in the surface. However, the lost carrier profile illustrated in Figure 10 should be rewritten under the consideration of surface etching effect. The re-calculated results are shown in Figure 45. The lost carrier re-calculated from the difference between the case of 0 Torr and that of 450 Torr in H_2 partial pressure shows double peaks as shown in Figure 44. Although the shallower peak can be well explained by the Mn accumulation the deeper peak cannot be explained only by Mn accumulation effect.

Moreover, Si redistribution in Chapter 5 is thought to be a result of a paring effect of Si_{Ga} donor and Mn_{Ga} accepter. At the same time Si_{Ga} and Si_{As} pair is to be existing also and the pair can move simultaneously as Mn_{Ga} moves. It is natural to think the ionized center make a paring because the binding energy of ionized center is lowering by paring of (+) and (-) centers. In our case the electron is provided by the reductive reaction at the surface, namely the etching occurs, resulted in the (+) ionized centers like Si_{Ga} is firstly attracted and then the Mn_{Ga}(-) and Si_{As}(-) are dragged as the paring. The deeper peak in lost carrier in figure 45 might be explained by the difference of distribution of these compensation centers. However, this interpretation is only presumption from the experimental facts and there is no evidence for direct proof.

Chapter 7

Evaluation of FET characteristics fabricated by using newly established annealing

7.1 Proposed new annealing method

A new annealing method for Si implanted GaAs is established under the consideration of the investigated results in this thesis. The standard annealing temperature and time is determined as 850 °C and 10 minutes. The ambient employed is $Ar/H_2/AsH_3$ mixture gas, each partial pressure is 600 Torr, 150 Torr and 3 Torr, respectively. Although it is better to adapt 100 % Ar/AsH_3 ambient in order to avoid an etching effect by H_2, the surface morphologies in the 100 % Ar/AsH_3 ambient sometimes degrade as non-mirror like in the case of inadequate purging time. In order to obtain mirror like surface a small amount of H_2 is effective with shorter purge time. There is no limitation for set up configuration and the perpendicularly set up of many wafers in the quarts cassette comes to be possible. By using Ar based annealing ambient the low cost annealing method is established with higher batch process and shorter through put..

7.2 Basic characteristics evaluated by FAT-FET

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In order to confirm the effect of $Ar/H_2/AsH_3$ annealing the FAT-FETs are fabricated using the simple MES FET process. FAT FET is a large dimension FET with a gate length of 100 μm and gate width of 100um so that it is very convenient to evaluate basic characteristics like g_m, Vp (pinch-off voltage), Ron and so on. The FAT FET is made by Si implantation into un-doped 2" GaAs with (100) surface. Si dose of $2 \times 10^{12}cm^{-2}$ / 100 keV for the channel and that of $2 \times 10^{12}\,cm^{-2}$ / 130 keV for the ohmic contact are implanted. The Au Schottky gate is deposited using evaporation and followed by the AuGe/Ni ohmic contact formation. The annealing condition is the newly established standard condition, namely 850 °C / 10 minutes. In order to compare the influence of the ambient both $Ar/H_2/AsH_3$ annealing and H_2/AsH_3 annealing in the FU/FF configuration are performed.

The results are summarized in Table 5. The average value of Vp is higher in $Ar/H_2/AsH_3$ annealing than that of H_2/AsH_3 annealing. This is directly reflected the difference of the activation ratio between $Ar/H_2/AsH_3$ and H_2/AsH_3 annealing. The standard deviation of the measured Vp in the H_2/AsH_3 annealing is about 300 mV and this value is relatively large. On the other hands, that of $Ar/H_2/AsH_3$ annealing is an order of 100 meV and considerably improved. Although so many causes are pointed out as for the origin of this Vp variation, most important factor is thought to be a dislocation distribution in the wafer. The dislocation has a cell-like structure and the As precipitates tend to gather in the dislocation. This excess As is said to be an origin of EL2 and the activation of implanted Si is high near the dislocation [48]. At the same time the impurities in crystal tends to concentrate on the dislocation. If the etching by H_2 enhances these impurities re-distribution as same as Mn case, it is understandable that the variation of Vp is enlarged by H_2 based annealing. The lower variation in Vp and the higher activation ratio helps the high speed operation of the integrated circuit. In the next Chapter, the results of the evaluation in high speed operation are described.

Table 5: Average Vp and its dispersion in each annealing conditions.

Sample No.	Carrier Gas	Set-up	P_{AsH3} (Torr)	Measuring Number (/ wafer)	Vp (V)	σ Vp (mV)
1-1	H_2	FU	3	1429	-3.15	314
2-1	H_2	FU	3	1413	-3.74	288
3-1	H_2	FU	3	1355	-2.88	254
1-2	Ar	FU	3	1472	-2.91	157
2-2	Ar	FU	3	1316	-3.6	102
3-2	Ar	FU	3	1382	-2.66	118

7.3 J-FET Fabrication Process

Figure 46 shows a brief fabrication process flow for the ion-implanted GaAs JFET. Firstly the channel region is formed by Si implantation with the dose of $3 \times 10^{12}\,cm^{-2}$ and the energy of 60 keV through the photo-lithography process (Figure 46(a)). After resist is removed, the ohmic region is formed by Si implantation with the dose of $3 \times 10^{12}\,cm^{-2}$ and the energy of 100 keV (Figure 46(b)). After removing the

resist, newly established $Ar/H_2/AsH_3$ annealing is performed. Then p-CVD Si_3N_4 passivation film with the thickness of 300 nm is deposited on the surface and the gate window is opened by the RIE (Reactive Ion Etching) using CF_4/O_2 mixture gas through photo-lithography process (Figure 46(c)). The resist is removed, then, Zn diffusion is performed with the condition of 600 ºC / 10min (Figure 46(d)). The Zn diffusion is controlled by the monitoring of P-N-P monitor. After Zn diffusion, gate metal of Ti/Pt/Au with the thickness of 50 nm/50 nm/200 nm is deposited by electron beam (e-beam) evaporation (Figure 46(e)) and the excess gate metal is etched off by the ion milling method through PR process (Figure 46(f)). Subsequently AuGe/Ni ohmic electrode is formed as shown in Figure 46(g). The ohmic contact is made by the alloy process with 400 ºC / 10 minutes in the forming gas followed by lift-off process. Then the dielectric film of SiO_2 with the thickness of 400 nm is deposited by p-CVD. The first interconnect metal of Ti/Au is deposited by e-beam evaporation after contact region is opened by CF_4/O_2 based RIE. It is etched off by ion milling after the photo resist is patterned (Figure 46(h)). If necessary, the second dielectric film of SiO_2 with the thickness of 500 nm are deposited and the second interconnect of Ti/Au is processed as same as the case with the first metal.

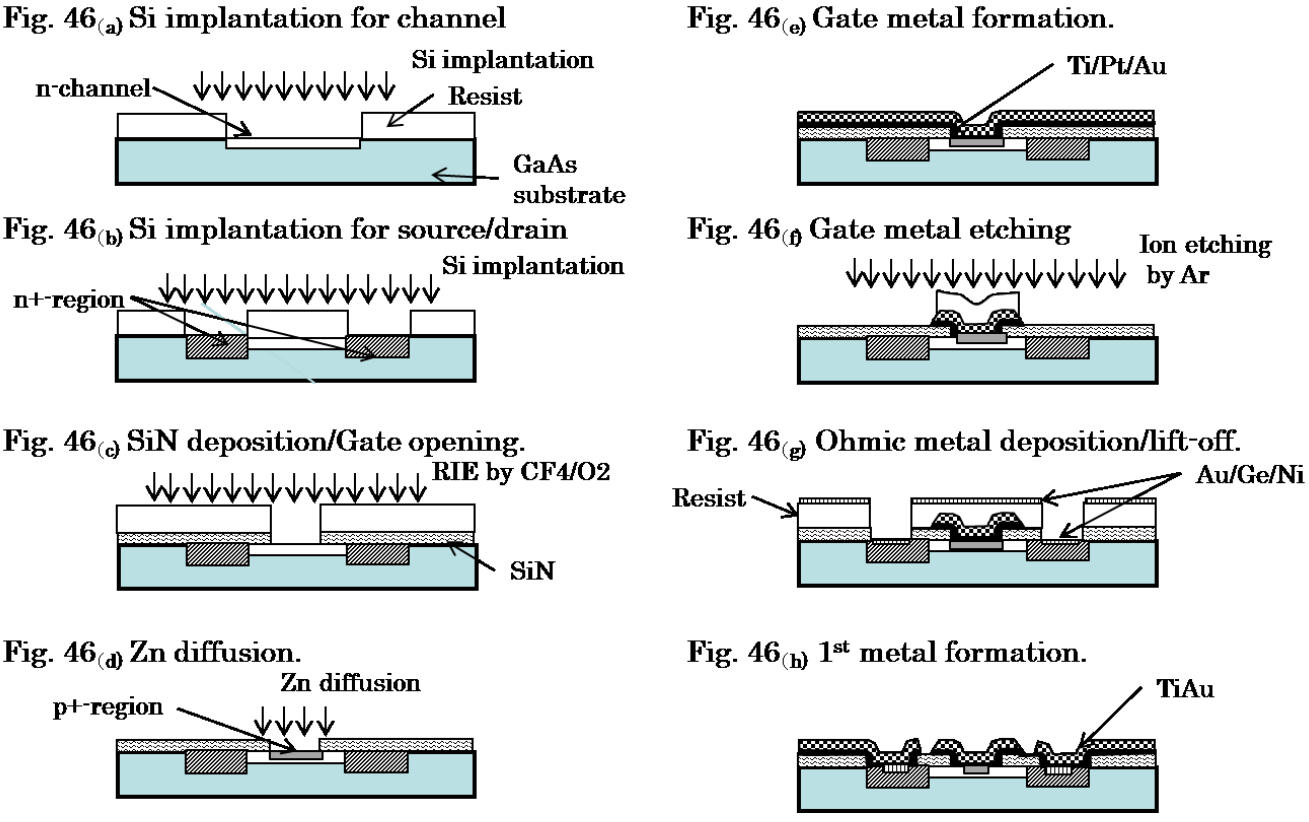

Figure 46: JFET fabrication flow.

Zn diffusion technique on to GaAs JFET using DEZ (Di-Ethyl Zinc) is firstly proposed by M. Dosen et. al. [12]. In this technique, diffusion coefficient is determined by the partial pressure of DEZ and maximum concentration of Zn accepter is almost constant at about $1 \times 10^{19}cm^{-3}$ as shown in Figure 47, therefore, the diffusion depth is easily determined by controlling the diffusion time as shown in Figure 48.

The JFET fabricated in this Chapter is controlled as to obtain enhancement type FET in order to compose high speed circuit based on DCFL (Direct Coupled FET Logic). The obtained typical current-voltage characteristic of the JFET is shown in Figure 49. The gate length and the gate width are 0.8 and 10 μm, respectively. The spacing between the n^+ contact layer and the gate contact is 0.5 μm. The drain current I_{ds} is 1.8 mA at the gate and at the drain voltage of 1 and 2 V, respectively. A trans-conductance g_m, as high as 340 mS/mm has been obtained. The average g_m, over a 3-inch wafer is 310 mS/mm at a Vth around +0.1 V. A maximum trans-conductance of 560 mS / mm has been measured by reducing the gate length to 0.35 μm in a JFET with a Vth of +0.3 V [49].

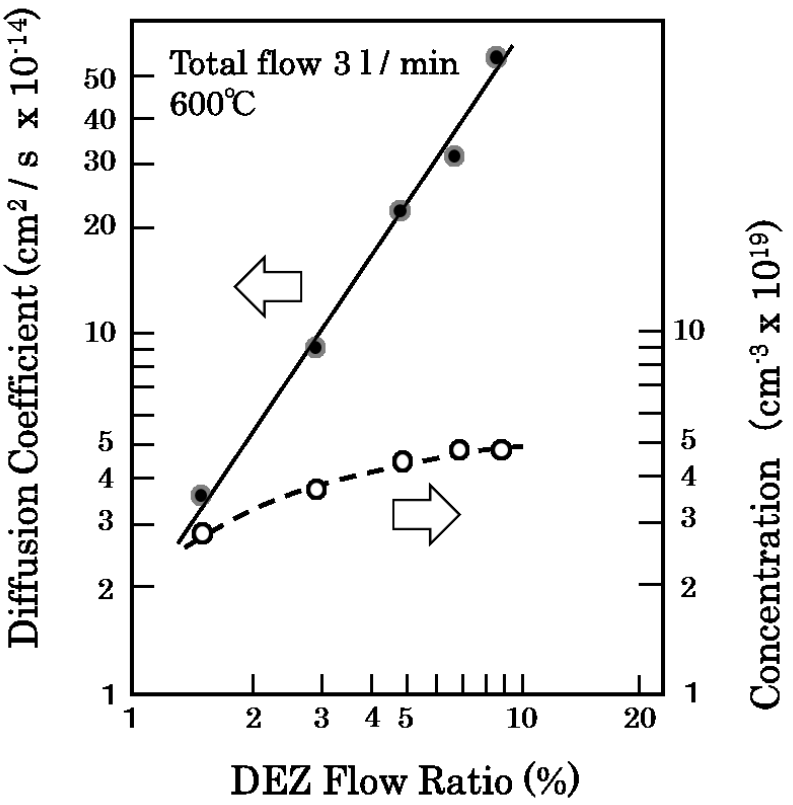

Figure 47: Diffusion coefficient and carrier concentration as a function of DEZ flow rate.

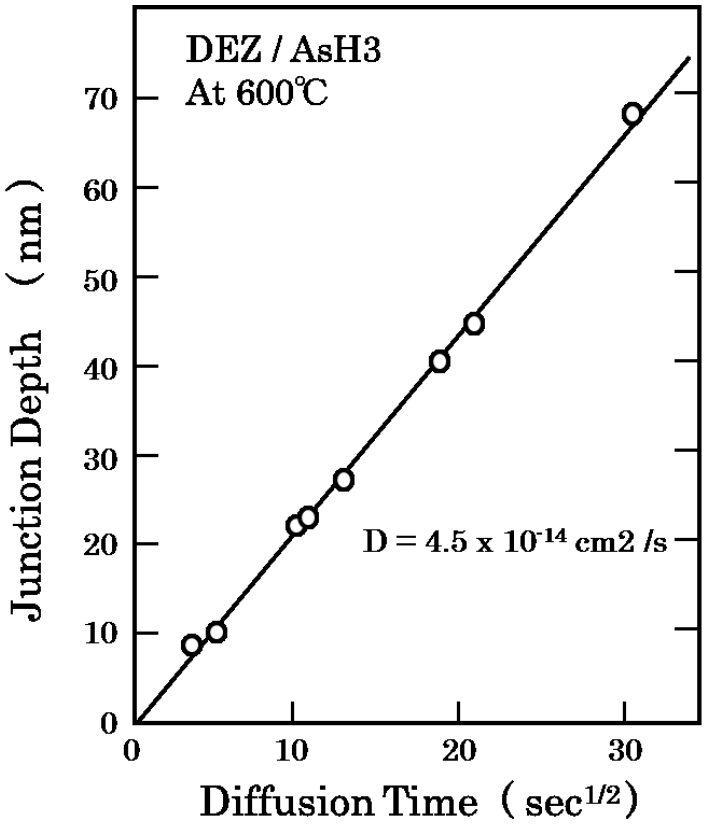

Figure 48: Junction depth as a function of the square root of the diffusion time at 600 °C with a flow ratio of 2 percent.

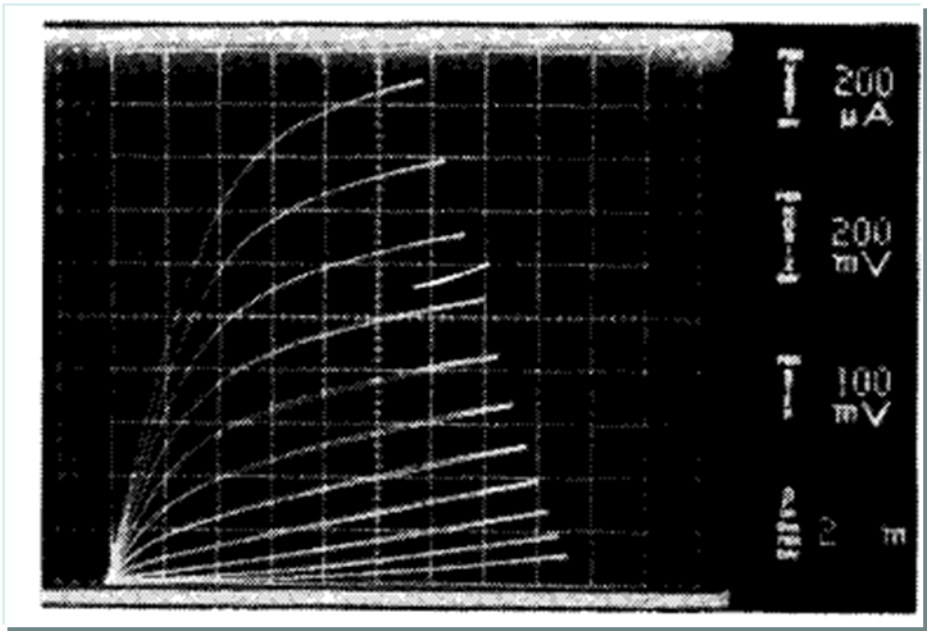

Figure 49: Current-voltage characteristics of the advanced J-FET. The gate length and the width were 0.8 and 10 μm, respectively.

7.4 Evaluation results of high speed circuits

The propagation delay time is evaluated with a 21-stage ring oscillator composed of an E/R-type DCFL circuit. The minimum propagation delay time τ_{pd} is 22 ps / gate with a power consumption Pd of 0.42 mW / gate. An estimated f_t from this result is about 45 GHz and this value proves the high potentiality of the developed JFET. The relationship between propagation delay time and a power consumption as a function of Lg is shown in Figure 50. Here, the dashed line is a simulation results based on the Shockley model. The obtained results are well accordance with the simulation.

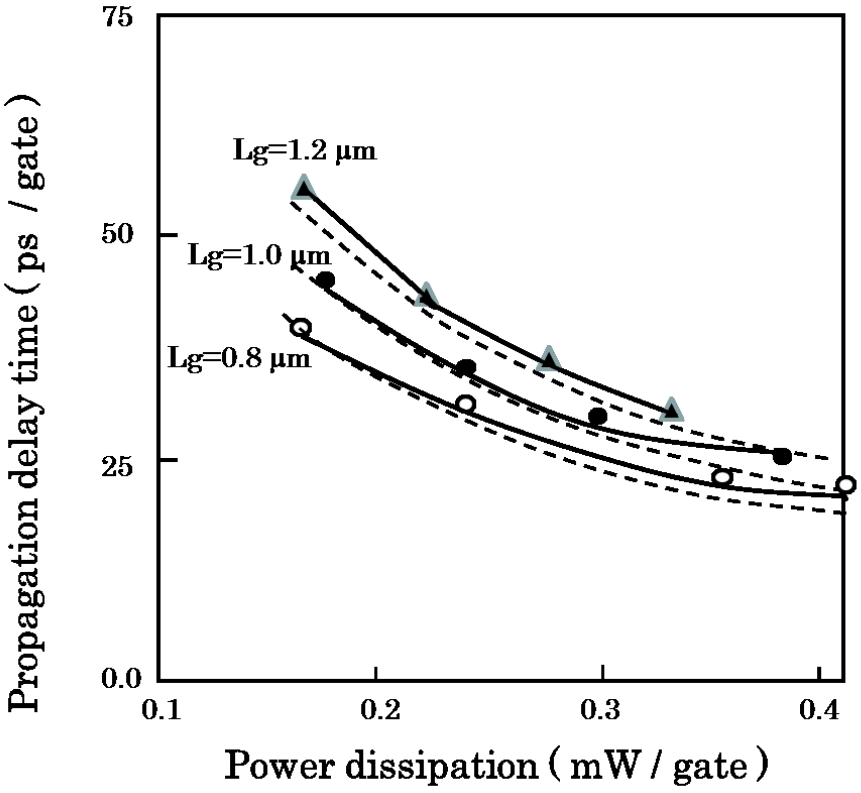

Figure 50: Relationship between propagation delay time and power dissipation as a function of gate length.

A divide-by-four static frequency divider is also fabricated with six NOR-type D-Flip-Flops (FF) showed in Figure 51 as the benchmark for a high-speed logic circuit. The load resistance of R_L is 1.3 kΩ in this circuit. The performance of the dividers is measured using a high-frequency on-wafer probing system with 50 Ω characteristic impedance. The maximum operating frequency of an input frequency of 6 GHz has been obtained. Input and output waveforms of the frequency divider at

6 GHz are shown in Figure 52. An output voltage swing of over 2.5 V can be obtained with a 50 Ω driving buffer and appears as 120 mV on the oscilloscope due to the attenuator and the probing system. The maximum toggle frequency is consistent with the expected frequency calculated by the result of the ring oscillator taking into account an average fan-out of 2.3. The power consumption per flip-flop is 20 mW at a supply voltage of 1.6 V. The maximum toggle frequency obtained by a JFET in this work is comparable to that of MESFET DCFL's. The power consumption is lower in the JFET DCFL than in the MESFET ever reported [50].

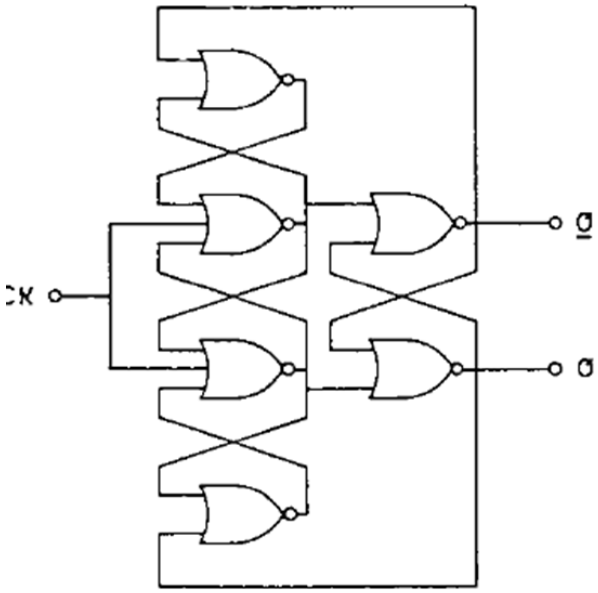

Figure 51: The logic diagram of the divide-by-four circuit.

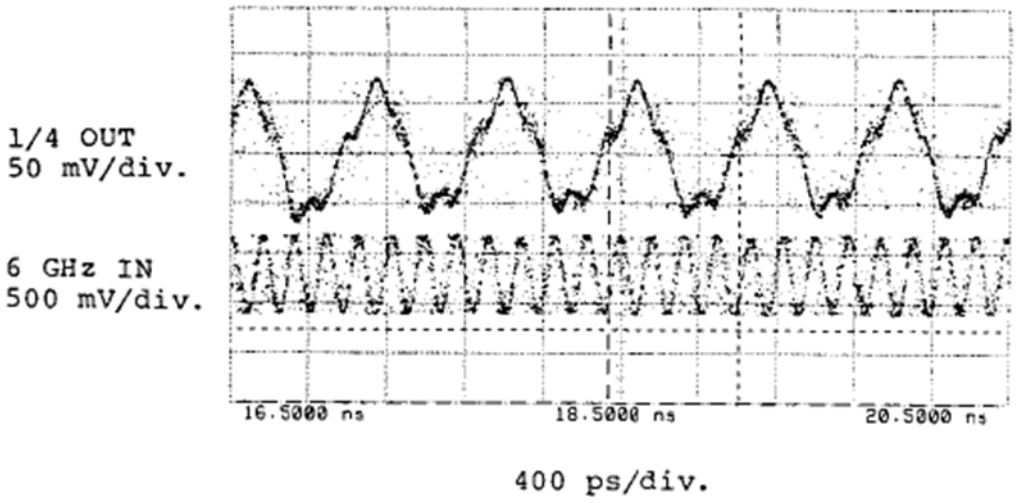

Figure 52: Operation wave forms of the divided-by-four logic circuit.

In conclusion, the applicability of GaAs JFET's to high-speed LSI's has been demonstrated. Both the high channel doping above $2 \times 10^{18}\,cm^{-3}$ and the shallow junction depth obtained by newly proposed $Ar/H_2/AsH_3$ annealing contributed to the high trans-conductance of 340 mS/mm, giving rise to the large current driving capability that is essential for high-speed circuits. A propagation delay time of 22 ps / gate is measured with a power consumption of 0.42 mW/ ate. By reducing the gate length to 0.4 μm, we have obtained a propagation delay time of 15.7 ps/gate with 0.51 mW/gate. This value corresponds to the f_T of 65GHz. A divide-by-four static frequency divider operated up to the input frequency of 6 GHz. It is confirmed that the GaAs JFET is more advantageous for high-speed LSI application than the MESFET since the JFET inherently has a larger noise margin by means of larger forward gate bias than the MESFET.

Chapter 8

Summary

A superior GaAs JFET is developed by investigating the basics of Si activation mechanism in ion-implanted GaAs. Especially in the channel formation process, it is found that not only the basic annealing conditions like temperature, time, sample set-up configuration and so on but also the ambient control addition to the As over pressure is essentially important. The carrier reduction in activation of implanted Si only in the ambient including H_2 is observed and it is confirmed by the photoluminescence study and SIMS analysis that the Mn_{Ga} acceptor accumulation is taken place near the surface. It is revealed that this Mn accumulation is caused by congruent etching in GaAs surface by means of H_2 - host As atom reaction and the etching is ruled over Ga evaporation. This fact is directly confirmed by the detection of AsH_3 in Q-mass analysis and the detection of Ga in PIXE analysis. Regarding the mechanism for the Mn_{Ga} accumulation during the high temperature annealing the Mn_{Ga}(-) / Si_{Ga}(+) or Mn_{Ga}(-) / Si_{Ga}(+) / Si_{As}(-) combined diffusion model is implied by the RBS/PIXE analysis. At this diffusion process it is also suggested that a kind of site transfer like a Si_{Ga} and Si_{As} does not play an important role in carrier loss near the surface by the RBS/PIXE analysis. The optimized annealing condition from the viewpoints of crystallographic investigation is determined using RBS/PIXE analysis. A newly proposed annealing conditions for Si implanted un-doped GaAs is 850 ºC in temperature, 10 minutes in time and $Ar/H_2/AsH_3$ mixture ambient with each partial pressure of 600 Torr, 150 Torr and 3 Torr, respectively. In this annealing condition any wafer set-up configuration is possible and this realizes remarkably excellent production capability.

By using this annealing condition, the FAT-FET is fabricated. It is confirmed that the higher activation of implanted Si and the lower variation of Vth than conventional H_2 based annealing is accomplished.

The GaAs JFET with the Lg of 0.8 μm is also fabricated using Zn diffusion technique. The maximum trans-conductance of 340 mS/mm and the fastest propagation delay time of 22 ps in 21-stages ring oscillator is obtained. Furthermore, by shorten the gate length to the 0.4μm the maximum trans-conductance of 560 mS / mm and the fastest propagation delay time of 15.7 ps are achieved. These values are corresponding to the f_T of 65 GHz and it means that the top class speed in the world is attained.

These remarkable progresses are made by the high carrier density and shallowness realizing in the channel. A newly proposed annealing technique based on basic investigations largely contributes to high speed operation and open a path to apply GaAs FETs to high speed and high frequency applications.

Chapter 9

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Appendix I

RBS/PIXE analysis on out diffusion of Ga and As atoms into the capping film of SiO_x and SiN_y.

A1 Basics of RBS / PIXE analysis

RBS (Rutherford Back-scattering spectrometry) is nondestructive nuclear method for elemental depth analysis of nm-to-mm thick films. It involves measurement of the number and energy distribution of energetic ions (usually MeV light ions such He+) backscattered from the atoms within the near-surface region of solid targets.

A projectile ion of the mass M1, atomic number Z1 and initial kinetic energy Ein penetrates the sample into the depth x, where elastically scatters from a target atom of the mass M2 and atomic number Z2 under the scattering angle θ, having kinetic energy Eout. The backscattered ion escapes from the sample with kinetic energy Escat. We have to take into account the energetic losses of ions Ein penetrating to the depth x and the energetic losses of ions Eout after elastic collision. Energy losses are described by linear stopping power Sp, which is a function of energy. A schematic view of this back scattering is shown in Figure A1.

θ Scattering angle
M1 Mass of incident ion
M2 Mass of target atom
K1 Atomic number of incident atom
K2 Atomic number of target atom
E Ion energy

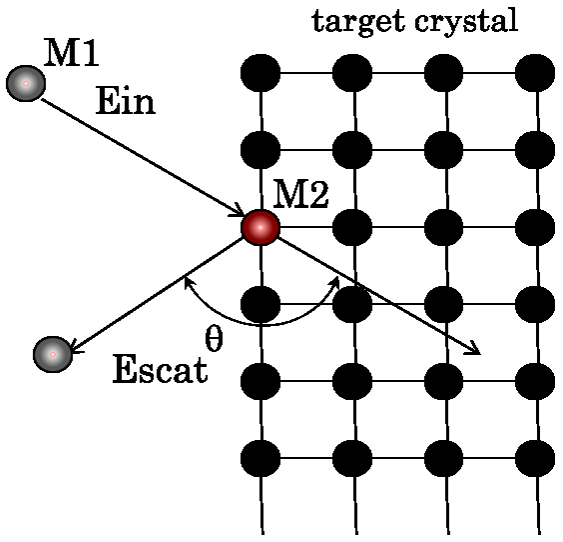

Figure A1: Schematic view of back scattering.

Considering the kinematics of the collision (that is, the conservation of momentum and kinetic energy), the energy Escat of the scattered projectile is reduced from the initial energy E0:

$$Escat = K\text{-}Ein \qquad (A1)$$

where k is known as the kinematical factor, and

$$K = \frac{E_{scattered}}{E_{incident}} = \left[\frac{\left(1 - \left(\frac{M_1 \sin\theta}{M_2}\right)^2\right)^{\frac{1}{2}} + \frac{M_1 \cos\theta}{M_2}}{1 + \frac{M_1}{M_2}} \right]^2 \qquad (A2)$$

The value of K in representative ions is shown in Figure A2.

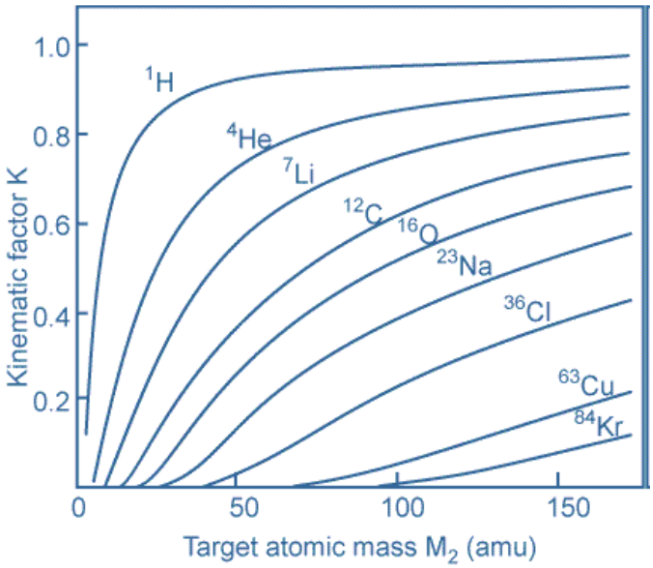

Figure A2: Kinematic factor of representive atoms.

RBS-channeling spectrometry enables to investigate crystalline materials. The signal of the impurity and host lattice in RBS spectra is separated by scattering kinematics. The angular yield curve (scan) is obtained by monitoring the yield of the impurity and host lattice along the channeling axis using ion beam impact angle changing. From the angular yield curves of the axial channels in material we obtain the impurity position in the measured crystallographic direction. In order to determine the lattice position of impurities several relevant crystallographic directions have been selected.

PIXE (particle-induced x-ray emission) can analyze the species of target atoms by analyzing the energy of characteristic x-ray emission. In PIXE the incident beam particles (usually 1-3 MeV protons) eject inner shell electrons from the target atoms

which results in the emission of characteristic X-rays. By using a suitable x-ray detector all the elements heavier than carbon can be detected in principle. Schematic view of simplified outlines of electron shell is showed in Figure A3. Therefor different atoms of near atomic number can be distinguished by the different characteristic x-ray emission.

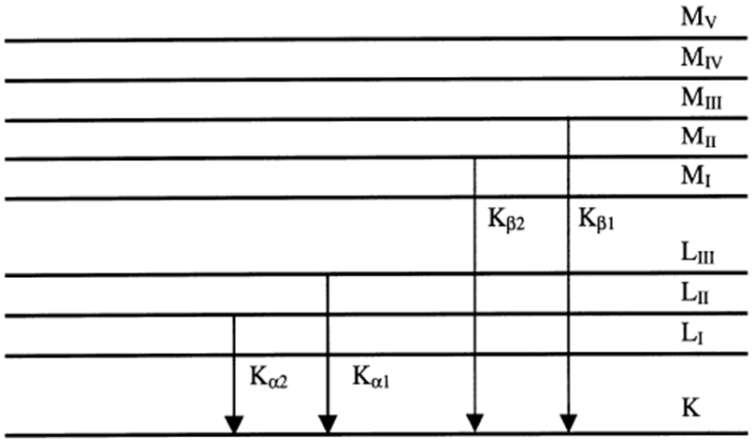

Figure A3: Schematic view of simpified outlines of orbitals in electron shell.

A2 Analysis on Ga and As out-diffusion in capped annealing

Residual Ga and As atoms in SiO_x and SiN_y dielectric films deposited on GaAs are investigated by RBS and PIXE analysis [18]. After carefully cleaning the surfaces, SiO_x films having a thickness of about 200 nm are deposited on these surfaces by using CVD methods at 400 °C using a conventional reactor. SiNy films having about the same thickness are also deposited by using p-CVD methods at 350 °C. Optical index of refraction and film thickness are measured by ellipsometry. The samples are annealed at a temperature between 850 and 900 °C (mainly at 850 °C) in a H_2 / AsH_3 ambient at an AsH_3 partial pressure 0f 0.75 or 12 Torr. The annealing time is varied from 2 to 50 minutes. Neither cracking nor peeling of the surfaces is observed after high-temperature annealing. Since the atomic weights of the substrate elements are higher than those of film elements, we have to do some contrivance on the samples to obtain more accurate results. Therefore, the self-supporting insulator films are prepared by completely etching off GaAs substrates using the etchant of $3H_2SO_4$, H_2O_2, H_2O. Schematic views of the self-supporting samples are shown in the insets in Figure A4. A typical diameter of the etching region is 3 mmϕ, which is sufficiently larger than the incident ion beam spot.

A typical RBS spectrum for a self-supporting SiO_x /GaAs sample is shown in Figure A4. The signals of Si and O atoms are well distinguished in the backscattered

energy spectrum. Moreover, the residual substrate atoms (Ga and/or As), which have probably diffused from the substrate into the dielectric film during deposition and/0r annealing, and have remained in the film after annealing, are also distinguished in the spectrum. Notice that the energy width of Si and O are not the same, which is attributed to the difference of the kinetic energy loss factors.

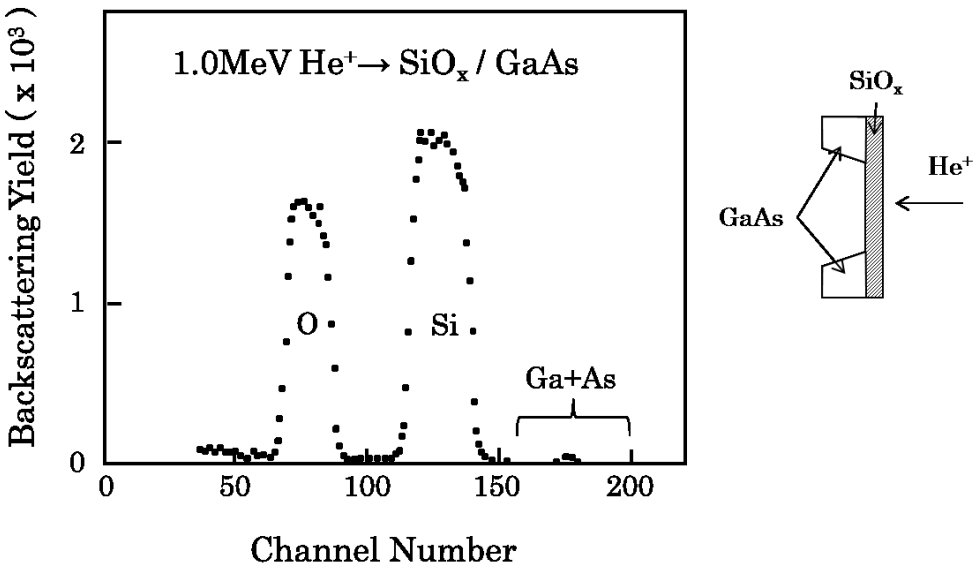

Figure A4: Typical RBS spectrum for a self-supporting SiO_x /GaAs.

Therefore, the energy width of out-diffused Ga and As atoms will appear wider than that of Si. We can also determine the atomic composition ratio at in the expression SiO_x and the content ratio of residual substrate atoms to Si in SiOx. And by comparing these spectra with a random RBS spectrum for crystalline Si, We can determine the absolute values of atomic densities of Si, O, and residual substrate atoms (Ga, As) in SiO_x films. This procedure is same in the case of SiN_y films and calculated values of X and Y are shown in Table A1. The value of 1.88 in SiO_x and 1.05 in SiN_y is slightly smaller than stoichiometric SiO_2 and Si_3N_4 respectively. However, the values have validity because the both films are including much H atoms when the Si source is SiH_4.

Table A1: Composition of the dielectric films.

Material	Si ($\times 10^{22} cm^{-3}$)	O or N ($\times 10^{22} cm^{-3}$)	Ratio
SiO_x (CVD)	2.17	O=4.07	x=1.88
SiN_y (p-CVD)	3.38	N=3.55	y=1.05

A typical PIXE spectrum of a self-supporting SiO_x/ GaAs sample is shown in Figure A5. The residual substrate atoms are well separated in the characteristic x-ray frame, and we can calculate the atomic concentration ratio of residual Ga and As atoms since self-absorption effects of x-rays and energy loss of proton beams in the samples are negligible by means of the thin thickness of SiO_x film.

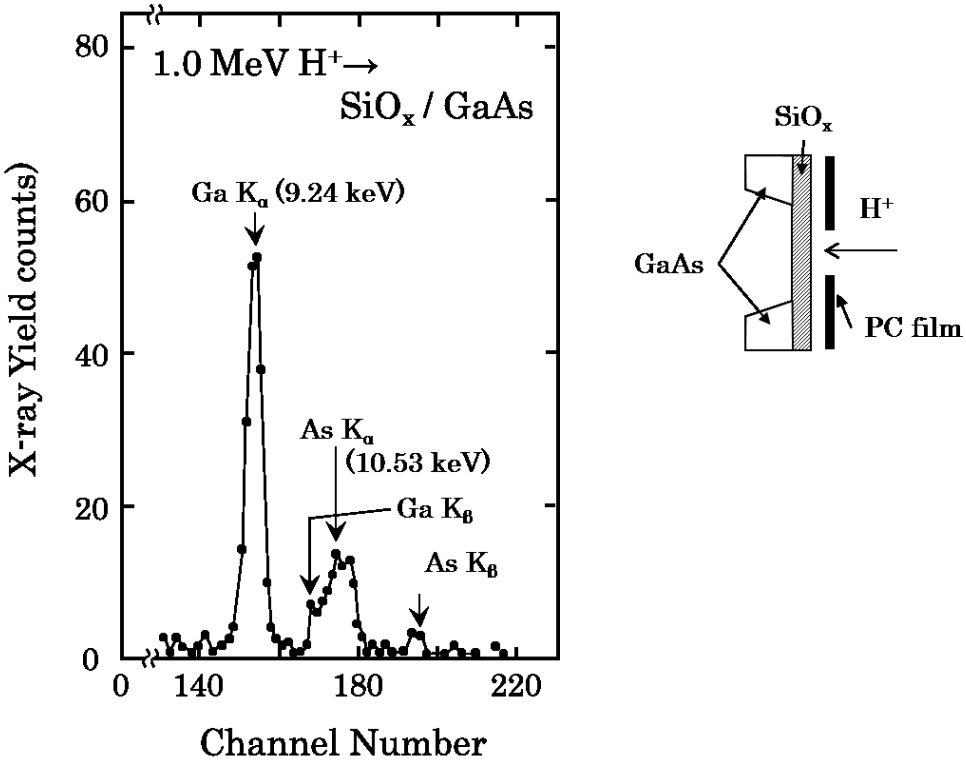

Figure A5: Typical PIXE spectrum of a self-supporting SiO_x/ GaAs.

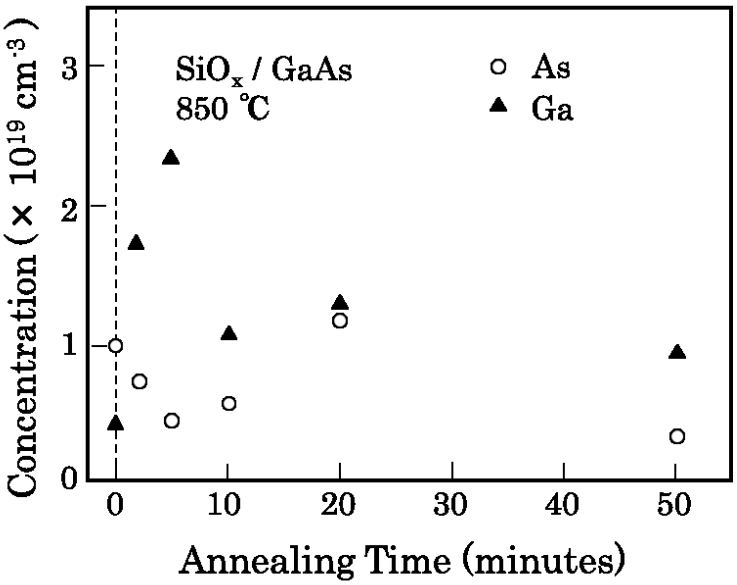

Figure A6: Dependence of out-diffused Ga and As atoms on annealing time in SiO_x/GaAs systems. Annealing temperature is 850 ºC.

The calculation details are described in ref. [18]. Here, only the results are shown in Figure A6. Individual Ga and As concentrations in the SiO_x films shows as a function of annealing time. The concentrations of residual atoms are written in the unit atoms/cm^3, which means the average value through the films. From Figure A4 and A6, we can see that in the insulating films of SiO_x/ GaAs systems, the residual Ga atoms prevail over the As atoms, in all annealed samples. These results are consistent with those previous reports quantitative1y [40, 41]. However, the mean value of residual substrate atoms is of the order of 10^{19} atoms/cm^3, and this value is comparable to that of SiN_y/ GaAs systems (see below). Moreover, no build-up of Ga atoms at the SiO_x surface could be found. Therefore, it may be an appropriate expression that even in SiO_x films, the number of out-diffused Ga atoms can be limited within a comparatively low level. Furthermore, notice that in the sample without annealing, Ga and As atoms are detected. (Only in this sample are As atoms slight1y dominant.) In addition, the concentrations of out-diffused Ga and As atoms have a maximum value at a specific annealing time for the post-annealed samples. These features are not explained by a simple diffusion model.

A typical RBS spectrum of a self-supporting SiN_y/ GaAs sample is in Figure A7. The signals of Si, N, and out-diffused substrate atoms are well separated from each other, as well as the spectrum of SiO_x/GaAs. In addition, a small peak between Si and N signals is found, which indicates oxygen at the surface. Except for the surface oxygen, we found no other oxygen in the films. Comparing the spectra with those of SiO_x /GaAs, Si and N signals have a wider width in the energy space, although both samples have almost the same film thickness. The difference is directly attributed to the atomic densities of the films and the resultant values of energy losses (stopping

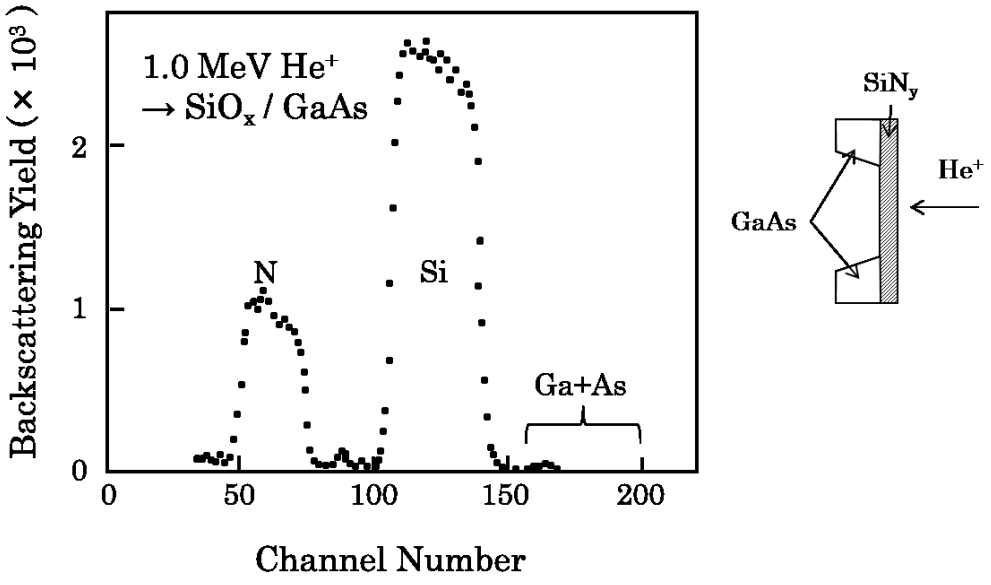

Figure A7: A typical RBS spectrum for a self-supporting SiN_y /GaAs.

powers) for incident H^+ ions. Using the same procedures shown in the case of SiO_x /GaAs, we can easily determine the absolute values of atomic densities for each element of the film and the absolute concentration of residual substrate atoms in the film. The obtained results on the composition ratio and the absolute atomic densities of SiN_y are shown in Table A1. In addition, we found no difference in these values on the post-annealed samples, as well as SiO_x/GaAs systems.

Moreover, for annealing at 850 °C in the H_2 /AsH_3 ambient at an AsH_3 partial pressure of 0.75 Torr, distributions of out-diffused atoms in the SiN_y films are investigated. The substrate atoms are detected in the interface region of the sample without annealing, as well as the as-deposited sample of SiO_x/GaAs. However, the profiles of residual substrate atoms in SiN_y films are not similar to those in SiO_x films. In brief, the peaks appearing in the interface regions grow with increasing annealing time, and the peak indicates the maximum value for the sample with an annealing time of 5 min. With increasing annealing time, the height of the peak decreases and then the width of the peak spreads in the whole region of the film. Finally, the distribution seems to approach a dynamical equilibrium state.

A typical PIXE spectrum for a self-supporting SiN_y / GaAs sample measured to distinguish out-diffused elements is shown in Figure A8. Generally, As_{Ka} peak is larger than Ga_{Ka} x-ray yields, contrary to SiO_x/GaAs systems, which means that

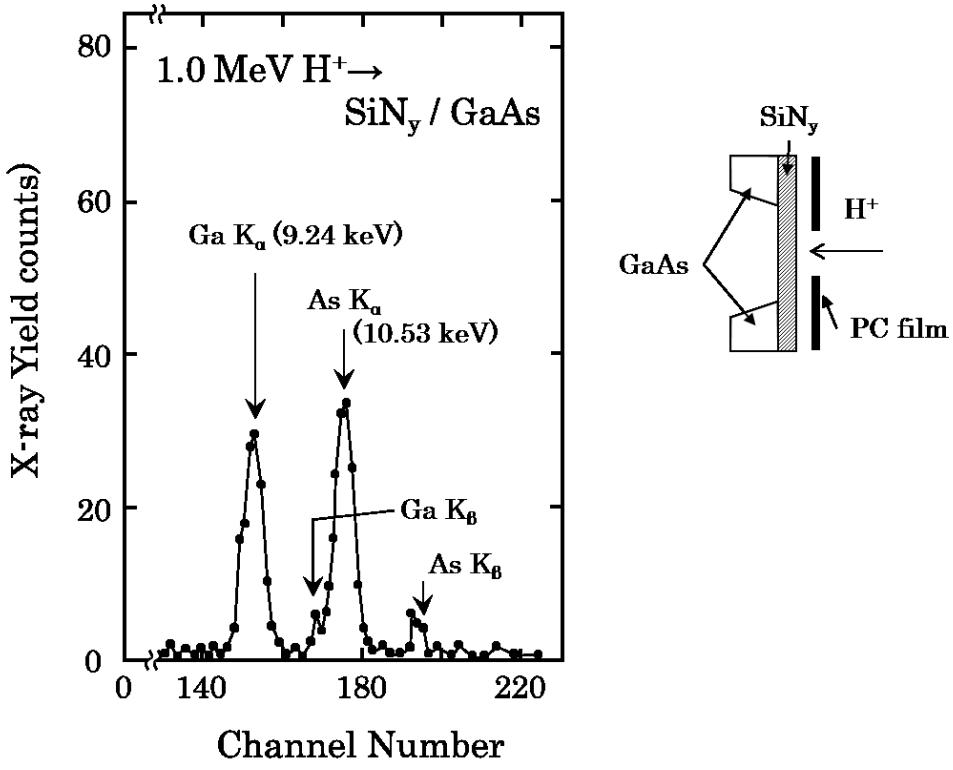

Figure A8: A typical PIXE spectrum of a self-supporting SiN_y/ GaAs.

out-diffused Ga atoms are suppressed and As atoms in the film are more dominant in the system. The summarized results for the SiN_y/GaAs system are shown in Figure A9 as a function of annealing time. From the Figure A6 and A9, we can see that in this case out-diffused Ga atoms are well suppressed compared with those of SiO_x films but, on the contrary, As atoms are detected and prevail over Ga atoms in all samples used in this experiment. On the other hand, the profiles of out-diffused atoms (mainly As atoms) in the SiN_y films have different shapes compared with those in SiO_x films.

Since accumulation of the substrate atoms in the interface region of the films is very conspicuous, it might be appropriate to regard these features as mixing or as a reaction between SiN, and GaAs rather than out-diffusion. In any case, as also shown in the results of SiO_x/GaAs systems, it is clear that aspects cannot be explained by a simple diffusion model.

It is evident in the experiments that the substrate atoms exist even in the as-deposited films without annealing in both SiO_x/GaAs and SiN_y/GaAs systems. That fact suggests that plasma and/or thermal damage leave a damaged layer (or a disordered layer) in the interface region of the substrate during the film deposition process itself. This damaged layer shown could be an initial diffusion source for Ga and As atoms. A specific annealing time in Figure A6 showing a maximum yield at a given annealing temperature can be mainly attributed to the damaged layer. Residual substrate atoms in SiO_x films increase with increasing annealing time and, after consuming the damaged layer, they decrease with further annealing

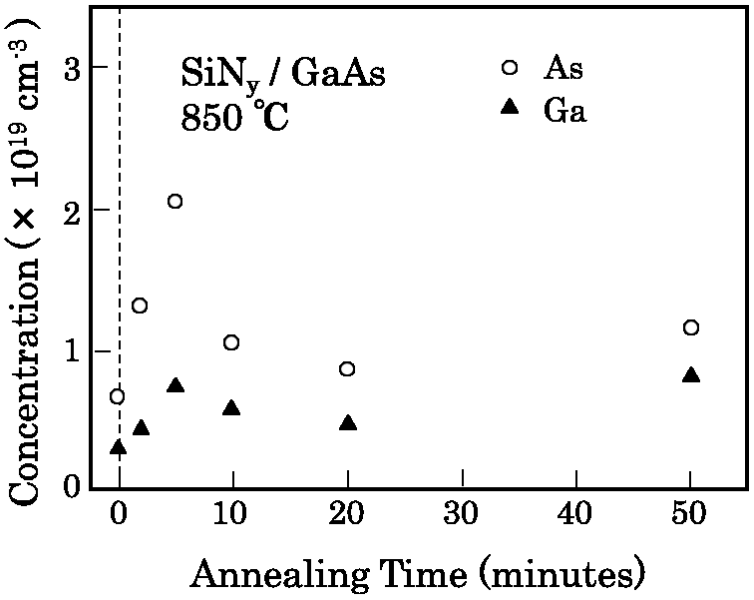

Figure A9: Dependence of out-diffused Ga and As atoms on annealing time in SiN_y/GaAs systems.

approaching to a dynamical equilibrium state. An annealing at higher temperature results in a shorter specific annealing time with lower maximum yield. These features are shown in Figure A10 for Ga in the SiO_x films. The larger diffusion constant [42, 43] at high temperature is probably responsible for the results.

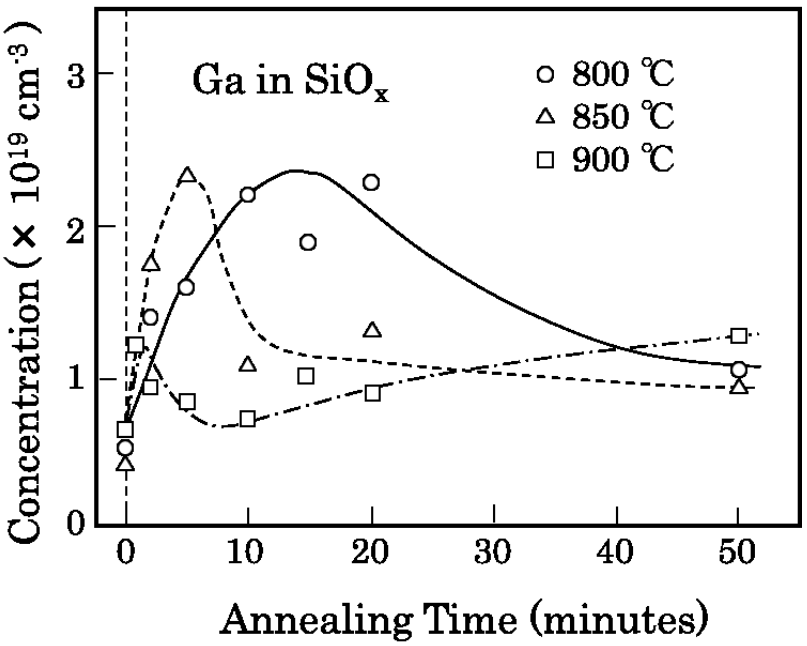

Figure A10. Residual Ga atoms in SiO_x films as functions of annealing time and annealing temperature.

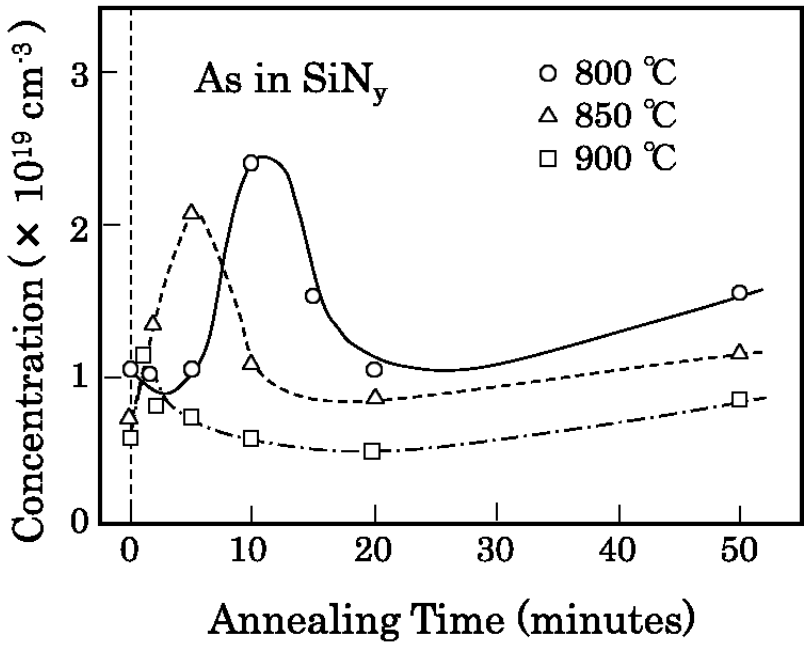

Figure A11 Residual As atoms in SiN_y films as functions of annealing time and annealing temperature.

Furthermore, the fact of showing maximum yield at a specific annealing time is the same in SiN_y /GaAs and SiO_x/ GaAs shown in Figure A6 and A9. Dynamic behavior of the residual substrate atoms in SiN_y films is thought to be, however, different from those in SiO_x films. Accumulation of the residual substrate atoms at the interfaces suggests that mixing of the layers or reaction at the interface between a SiN_y film and the damaged GaAs layer dominates out-diffusion of the substrate atoms. The As content in the SiN_y film is shown in Figure A11 at various annealing temperatures. Reaction or mixing at the interface can be enhanced by higher annealing temperature and the damaged layer can be consumed within a shorter period giving rise to a shorter specific time for lower maximum yield. Here, we should notice that SiO_x films are deposited by thermal CVD at 400 °C (It is higher than that of SiN_y) and SiN_y films are deposited by plasma-CVD at 350 °C. From this fact, there is a possibility that the damaged layer in SiO_x films tend to be Ga rich at the surface by higher growth temperature and the damaged layer in SiN_y films tend to be more disordered by the attacking of plasma. These interpretations well explain the results of this time out-diffusion of residual substrate atoms.

The results of As overpressure annealing support the damaged layer model. The concentrations of residual Ga and As atoms and the ratio of the As content to the Ga one are summarized in Table A2 for 10 min annealing in AsH_3 overpressure of 0.75 Torr and 12 Torr at 800 °C. Total residual concentration of Ga and As drastically decreases at higher As overpressure in the both systems. However, the As/Ga ratio increases in SiO_x /GaAs systems suggesting a barrier of As overpressure on out-diffusion of Ga. On the contrary, the As/Ga ratio decreases in SiN_y/GaAs systems, which suggest suppression of As out-diffusion in mixing or reaction layer at the interface. The As overpressure acts as keeping a stoichiometric composition in the interface of both encapsulation systems. However, this results shows the capping films of SiO_x or SiN_y are not complete barrier for the protection of dissolution in GaAs surface during the high temperature annealing and it is found the host atoms out-diffuse penetrating through the capping films.

Table A2 Influence of As overpressure on residual Ga and As atoms.

Cap Structure	P_{AsH3}	Ga	As	Total	Ratio
	(Torr)	($\times 10^{19} cm^{-3}$)	($\times 10^{19} cm^{-3}$)	($\times 10^{19} cm^{-3}$)	(As/Ga)
SiO_x / GaAs	0.75	2.20	0.60	2.80	0.30
	12.0	1.25	0.65	1.90	0.50
SiN_y / GaAs	0.75	0.85	2.35	3.20	2.80
	12.0	0.65	1.55	2.20	1.60

Thus, the capping annealing method is thought to be largely affected by the characteristics in the interface of cap films and GaAs. In any case, some factors at the interface dominate the out-diffusion of the substrate atoms through the film in SiO_x/GaAs and SiN_y/GaAs systems. Generally speaking, the nature of the SiO_x or SiN_y films deposited by thermal CVD or plasma-CVD is very sensitive to the various growth conditions like a temperature, gas source, initial surface state, power and so on. Therefore, less-damaged interfaces are expected to obtain suitable dielectric for encapsulation or passivation on GaAs.